Active antenna detector

SPECIFICATION

1 FEATURES

- TSMC SiGe BiCMOS 0.18 um
- Wide range of threshold adjustment
- A load current limit
- Portable to other technologies (upon request)

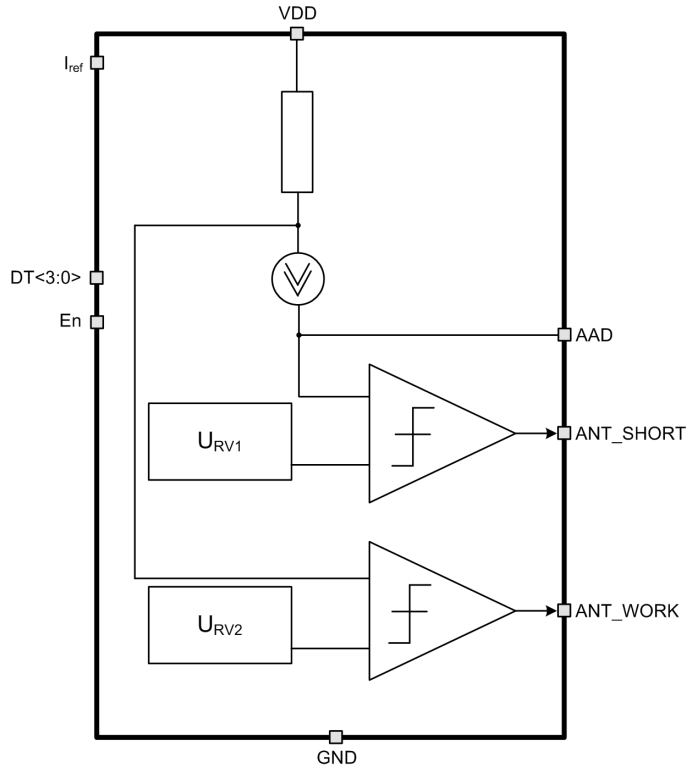
2 APPLICATION

- Receivers

3 OVERVIEW

The antenna detector supplies an active antenna and is able to detect both open and short circuits. A current limiter restricts the antenna current to a safe level in the case of a short circuit in order to protect the circuit.
The block is fabricated on TSMC018 SiGe technology.

4 STRUCTURE



U_{RF} – Reference voltage source

Figure 1: Active antenna detector structure

5 PIN DESCRIPTION

Name	Direction	Description
I_{ref}	I	Reference current
DT<3:0>	I	Digital code defined the active antenna nominal current
AAD	IO	Active antenna supply voltage
ANT_WORK	O	Active antenna status
ANT_SHORT	O	
EN	I	Enable/disable
VDD	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

Active antenna detector dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	220	µm
Width	561	µm

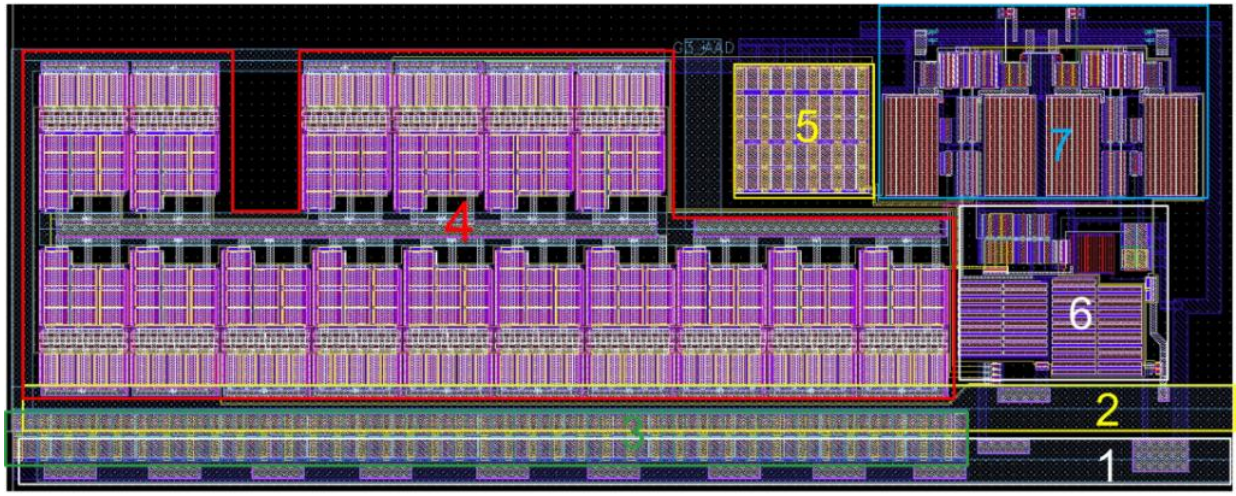


Figure 2: Active antenna detector layout

1. Ground bus
2. Supply voltage bus
3. Supply voltage filter
4. Active antenna current source
5. Reference voltage filter
6. Reference voltage source
7. Comparators

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC SiGe BiCMOS 0.18 um
Status _____ silicon proven
Area _____ 0.15 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 ÷ 3.6 V and Ta = -40 ÷ +85°C. Typical values are at V_{cc} = 3.3 V, Ta = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.8	3.3	3.6	V
Operating temperature range	Ta	-	-40	+27	+85	°C
Supply current	I_{cc}	-	-	140	-	µA
Detection current	I_{AW}	-	-	0.5×I_{nom}*	-	mA
Short circuit protection current	I_{AS}	In case of the short circuit	-	2×I_{nom}*	-	mA
Stand-by current	I_{stb}	-	-	-	25	nA
Input logic-level high	V_{IH}	For digital inputs EN, DT<3:0>	0.7V_{cc}	-	V_{cc}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Note: * – nominal current of an active antenna is set by the digital code DT<3:0>.

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation