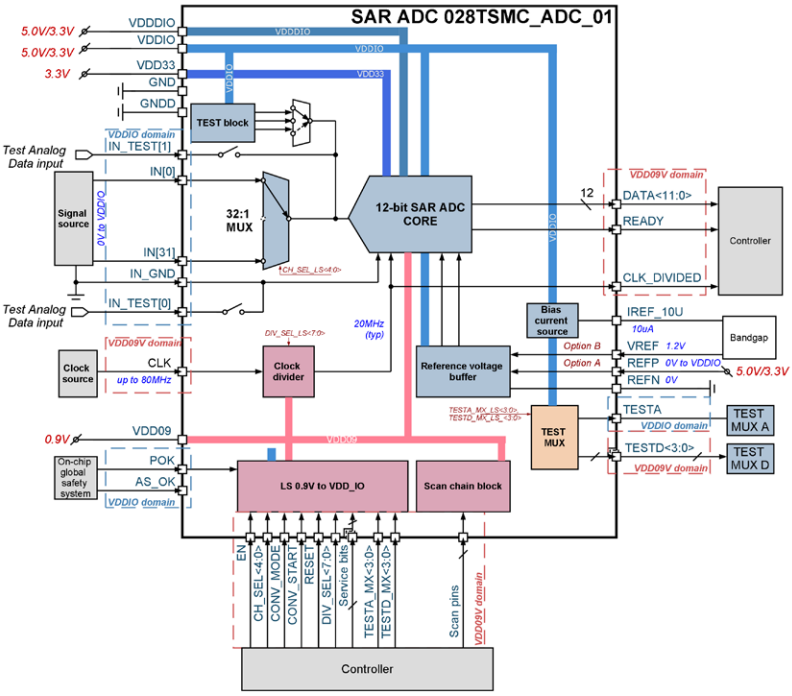
12-bit 1-channel up to 1.25MSPS SAR ADC

OVERVIEW

028TSMC_ADC_01 is a 12-bit 1-channel successive-approximation-register (SAR) analog to digital converter (ADC) with sample rates up to 1.25 MSPS.
The IP includes an analog multiplexer with 32 inputs to be driven into the ADC.
The IP block has a reference voltage buffer for the ADC.
028TSMC_ADC_01 operates directly from VDDIO/VDD33/VDD09 supplies.
Analog voltage references can be generated from internal buffer or supplied externally.

IP technology: TSMC eFlash 28nm.
IP status: in silicon verification.
Silicon area: 0.277mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	VDDIO	Option 5V		4.5	5.0	5.5	V
		Option 3.3V		2.97	3.3	3.63	
	VDD33	-		3	3.3	3.63	
Digital supply voltage	VDDDIO	Option 5V		4.5	5.0	5.5	V
		Option 3.3V		2.97	3.3	3.63	
	VDD09	-		0.81	0.9	0.98	
Operating junction temperature range	T_j	-		-40	25	150	°C
Full scale input	F_{SR}	-		-	VDDIO	-	V
Operating input range	A_{IN}	-		0	-	VDDIO	V
Reference voltage	V_{ref}	-		-	1.2	-	V
Resolution	N	-		-	12	-	bits
Sample rates	Fs	-		-	1.25	-	MSPS
External clock frequency	F_{CLK}	Contains internal clock divider		-	80	-	MHz
Operating clock frequency	F_{CLK_IN}	F_{CLK_IN} = 16 Fs		-	20	-	MHz
Total current consumption	I_{CC}	Fs=1.25MSPS	VDDIO=5V	-	1.1	1.32	mA
			VDDIO=3.3V	-	0.974	-	mA
Differential non-linearity	DNL	No missing code		-	±1	-	LSB
Integral non-linearity	INL	No missing code		-	±3	-	LSB
Spurious-Free Dynamic Range	SFDR	Fs=1.25MSPS, Fin=107kHz	VDDIO=5V	-	76	-	dB
			VDDIO=3.3V	72	75	-	
		Fs=1.25MSPS, Fin=517kHz	VDDIO=5V	-	75	-	
			VDDIO=3.3V	62	71	-	
Signal to noise ratio	SNR	Fs=1.25MSPS, Fin=107kHz	VDDIO=5V	-	66	-	dB
			VDDIO=3.3V	62	66	-	
		Fs=1.25MSPS, Fin=517kHz	VDDIO=5V	-	66	-	
			VDDIO=3.3V	61	65	-	
ENOB	ENOB	Fs=1.25MSPS, Fin=107kHz	VDDIO=5V	-	10.5	-	bit
			VDDIO=3.3V	9.8	10.5	-	
		Fs=1.25MSPS, Fin=517kHz	VDDIO=5V	-	10.5	-	
			VDDIO=3.3V	9.7	10.3	-	