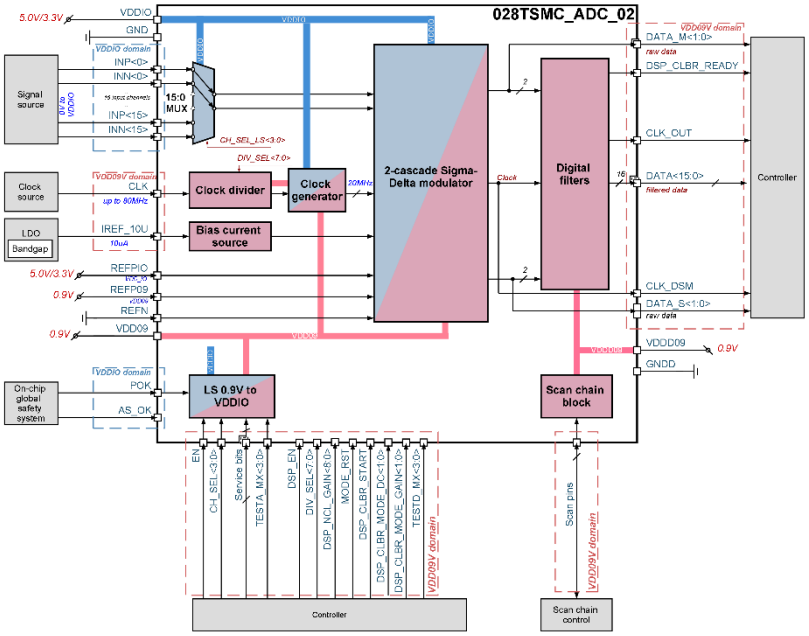
16-bit 2-channel 312.5kSPS delta-sigma ADC

OVERVIEW

028TSMC_ADC_02 is analog ADC based on 4th-order sigma-delta modulator with fully differential/single-ended signal processing. Second order discrete time Sigma-Delta stage includes two discrete time integrators, which are implemented using switch-capacitor (SC) technique, SC summing stage and 3-level quantizer.
ADC allows to obtain 92dB SNR at bandwidth 150kHz.

IP technology: TSMC eFlash 28nm.
IP status: pre-silicon verification.
Silicon area: 0.333mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	VDDIO	Option 5V		4.5	5.0	5.5	V
		Option 3.3V		2.97	3.3	3.63	
	VDD09	-		0.81	0.9	0.99	
Digital supply voltage	VDDD09	-		0.81	0.9	0.98	V
Operating junction temperature range	T_j	-		-40	25	150	°C
Full scale input	A_{IN}	Differential. Option 5V		-	10	-	V
		Single-ended. Option 5V		-	5	-	
Reference voltage	VREFP_IO	REFP_IO		-	VDDIO	-	V
	VREFP09	REFP09		-	VDD09	-	
	VREFN	REFN		-	GND	-	
Common mode voltage	Vcom	Option 5V		-	2.5	-	V
		Option 3.3V		-	1.65	-	
Reference current	I_{REF}	-		-	10	-	uA
Resolution	N	-		-	16	-	bits
Sample rates	Fs	-		-	312.5	-	kSPS
Bandwidth	BW	-		-	150	-	kHz
External clock frequency	F_{CLK_IN}	-		-	80	-	MHz
Operating clock frequency	F_{CLK}	-		-	20	-	MHz
Input clock frequency jitter (RMS)	Jclk	-		-	5	-	ps
Current consumption	I_{CC}	@VDDIO	Option 5V	-	0.9	1.1	mA
			Option 3.3V	-	0.6	0.7	
		@REFPIO		-	0.1	0.2	
		@VDD09		-	1.1	1.2	
		@VDDD09		-	0.3	1.5	
Spurious-Free Dynamic Range	SFDR	BW = 150kHz, Fin = 20kHz	Option 5V	75	88	-	dB
			Option 3.3V	74	80	-	
Signal to noise ratio	SNR	BW = 150kHz, Fin = 20kHz	Option 5V	87	92	-	dB
			Option 3.3V	85	87	-	
Signal-to-noise-and-distortion ratio	SINAD	BW = 150kHz, Fin = 20kHz	Option 5V	74	87	-	dB
			Option 3.3V	70	78	-	