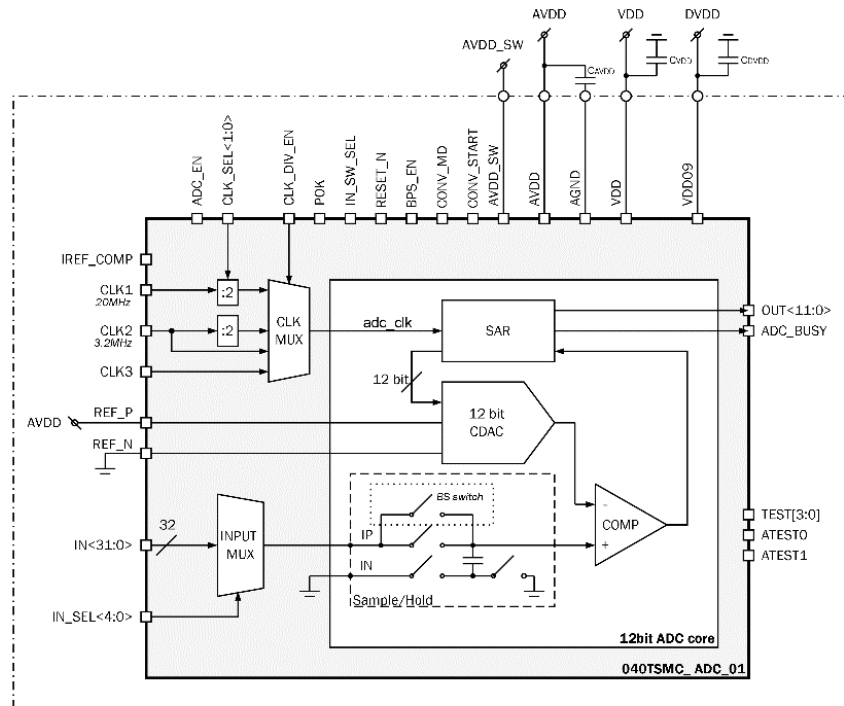


12-bit ultra-low power single-ended SAR ADC

OVERVIEW

040TSMC_ADC_01 is 12-bit analog to digital converter (ADC) with single-ended input of sample rates up to 1MSPS. The ADC supports a wide range of input clock frequency from 32kHz to 20MHz. The ADC operates with a 1.62V – 3.63V reference and includes a 12-bit successive approximation register (SAR) with inherent sample-and-hold. IP technology: TSMC 40nm CMOS technology. IP status: silicon proven. Area: GDS value 0.15 mm².



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units	
			Min	Typ	Max		
Operating temperature range	T _j	-	-40	+27	+85	°C	
Analog supply voltage	AVDD	-	1.62	-	3.63	V	
Digital supply voltage	DVDD	-	0.81	0.9	0.99	V	
Supply voltage	VDD	-	0.45	-	0.90	V	
Differential reference voltage	V _{ref}	REF	0	-	AVDD	V	
Current consumption	I _{CC}	F _{SR} = 1MSPS	3.3V@AVDD sw	-	140	170	μA
			1.8V@AVDD sw	-	80	90	
		F _{SR} = 100kSPS	@DVDD	-	25	30	μA
			3.3V@AVDD sw	-	18	28	
		@DVDD	-	4	6		
Shutdown current	I _{SD}	-	-	25.48	287.62	nA	
Full scale input	V _{full}	-	-	V _{ref}	-	V	
Operating input range	V _{IN}	-	0	-	V _{ref}	V	
Resolution	N	-	-	12	-	bits	
Sample rates	F _{SR}	-	1	100	1000	kSPS	
Offset error	E _O	-	-16	-	+16	mV	
Differential non-linearity	DNL	-	-	-	±1.1	LSB	
Integral non-linearity	INL	-	-	-	±3.3	LSB	
Signal-to-noise and distortion ratio	SINAD	AVDD=3.3B	F _{SR} = 1MSPS	60	63	-	dB
			F _{SR} = 100kSPS	63	65	-	dB
		AVDD=1.8B	F _{SR} = 1MSPS	47	59	-	dB
			F _{SR} = 100kSPS	65	67	-	dB
Spurious-free dynamic range	SFDR	AVDD=3.3B	F _{SR} = 1MSPS	64	69	-	dBc
			F _{SR} = 100kSPS	68	70	-	dBc
		AVDD=1.8B	F _{SR} = 1MSPS	50	61	-	dBc
			F _{SR} = 100kSPS	70	71	-	dBc
External clock frequency	F _{CLK}	-	0.032	-	20	MHz	
Startup time	t	C _{AVDD} = 10nF	-	-	20	μs	