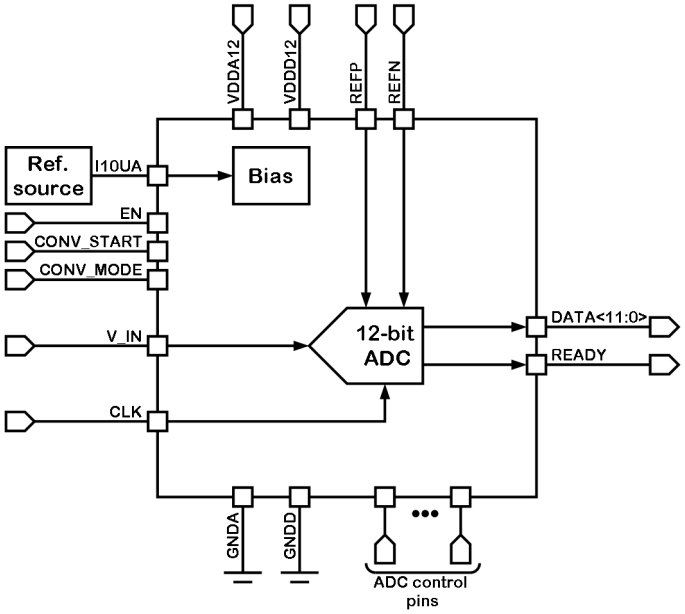
12-bit 1-channel up to 1 MSPS low power SAR ADC

OVERVIEW

055GF_ADC_02 is a low power 12-bit 1-channel ADC that uses a SAR architecture. The block consists of SAR ADC core and bias block The ADC settings allow you to put the block into standby mode.

IP technology: GF Embedded EEPROM 55nm technology.
IP status: silicon proven.
Silicon area: 0.12 mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	VDDA12	-	1.14	1.2	1.26	V
	VDDD12	-	1.14	1.2	1.26	
Operating temperature range	T_j	-	-40	+27	+85	°C
Current consumption	I_{VDDA}	F_S = 1 MSPS	-	335	-	uA
	I_{VDDD}		-	25	-	
	I_{REFP}		-	525	-	
Reference current	Iref	-	-	10	-	uA
Resolution	N	-	-	12	-	bit
Clock frequency	F_{CLK}	-	-	-	16	MHz
Sampling rate	F_S	-	-	-	1	MSPS
Input voltage	V_{IN}	-	0	-	VREFP	V
Differential reference voltage	VREFP	-	-	VDDA12	-	V
	VREFN	-	-	GNDA	-	V
Duty cycle	S	-	45	50	55	%
Spurious-free dynamic range	SFDR	F_{IN} = 104.5 kHz; F_S = 1 MSPS	-	76	-	dB
Signal to noise ratio	SINAD		-	65	-	dB
Effective number of bits	ENOB		-	10.5	-	bits
Differential nonlinearity	DNL		-	±1	-	LSB
Integral nonlinearity	INL		-	±3	-	LSB
Input logic-high level	V_{IL}	For digital inputs	0	-	0.2*VDDD12	V
Input logic-low level	V_{IH}		0.8*VDDD12	-	VDDD12	
Output logic-high level	V_{OL}	For digital outputs	0	-	0.4	V
Output logic-low level	V_{OH}		VDDD12-0.4	-	VDDD12	