12-bit 2-channel 50 - 125 MSPS pipeline ADC

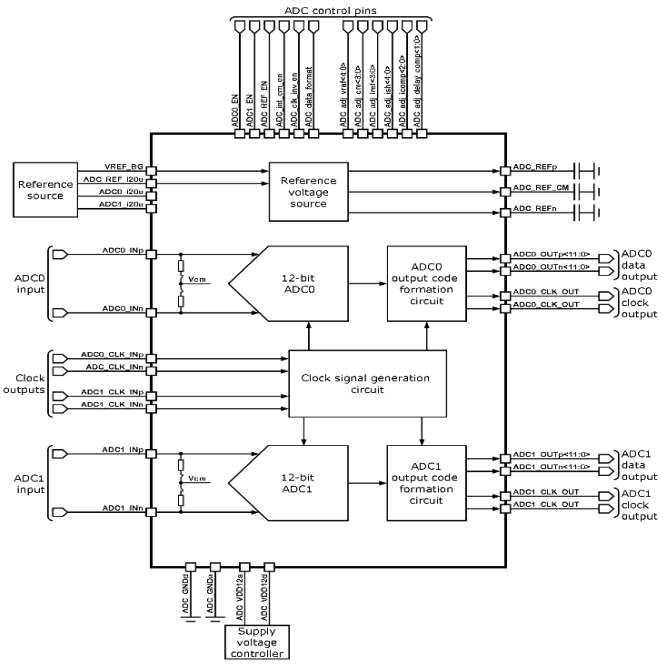
OVERVIEW

055TSMC_ADC_03 is a low power 2-channel 12-bit ADC based on a high-performance pipelined architecture. The block consists of 2 ADC cores, a clock signal generation circuit, an output code generation circuit and a reference voltage source. Separate power supply of the analog and digital circuits is implemented. The ADC settings allow to switch the block (or one of the channels) to standby mode.

IP technology: TSMC CMOS 55nm

IP status: silicon proven

Area: 3.5mm^2



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Unit
Analog supply voltage	V_{DDA}	-		1.08	1.2	1.32	V
Digital supply voltage	V_{DDD}	-		1.08	1.2	1.32	V
Operating temperature range	T_J	-		-40	+25	+110	°C
Current consumption	I_{DD}	V_{DDA} + V_{DDD}, two channels	@50 MSPS	170	172	177	mA
			@100 MSPS	225	228	234	
			@125 MSPS	260	264	269	
		Standby mode		-	9.5	-	µA
Power consumption	P_{TOTAL}	V_{DDA} + V_{DDD}, two channels	@50 MSPS	204	206	212	mW
			@100 MSPS	270	273	281	
			@125 MSPS	312	317	323	
Differential reference voltage	V_{REFP}	-		-	0.85	-	V
	V_{REFN}	-		-	0.35	-	
Input signal DC component	V_{CM}	-		-	0.6	-	V
Sampling rate	F_S	Minimum		10	50	-	MSPS
		Maximum		-	125	150	
Bandwidth	BW	-		-	400	-	MHz
Differential peak-to-peak input voltage range	$A_{IN(p-p)}$	-		-	1	-	V
Input clock duty cycle	S_{CLK}	-		45	50	55	%
Spurious free dynamic range	SFDR	Fin = 10.7 MHz	@50 MSPS	73.2	76.5	80.0	dB
			@100 MSPS	73.0	75.5	78.2	
			@125 MSPS	71.5	73.1	75.5	
Signal to noise ratio	SNR	Fin = 10.7 MHz	@50 MSPS	61.8	62.5	63.0	dB
			@100 MSPS	59.9	60.5	61.0	
			@125 MSPS	59.1	60.0	60.8	
Signal-to-noise and distortion ratio	SINAD (SNDR)	Fin = 10.7 MHz	@50 MSPS	-	61.1	-	dB
			@100 MSPS	-	60.9	-	
			@125 MSPS	-	59.5	-	
Effective number of bits	ENOB	Fin = 10.7 MHz	@50 MSPS	-	9.90	-	bit
			@100 MSPS	-	9.82	-	
			@125 MSPS	-	9.58	-	