10-bit 1-channel 10 – 150 MSPS SAR ADC

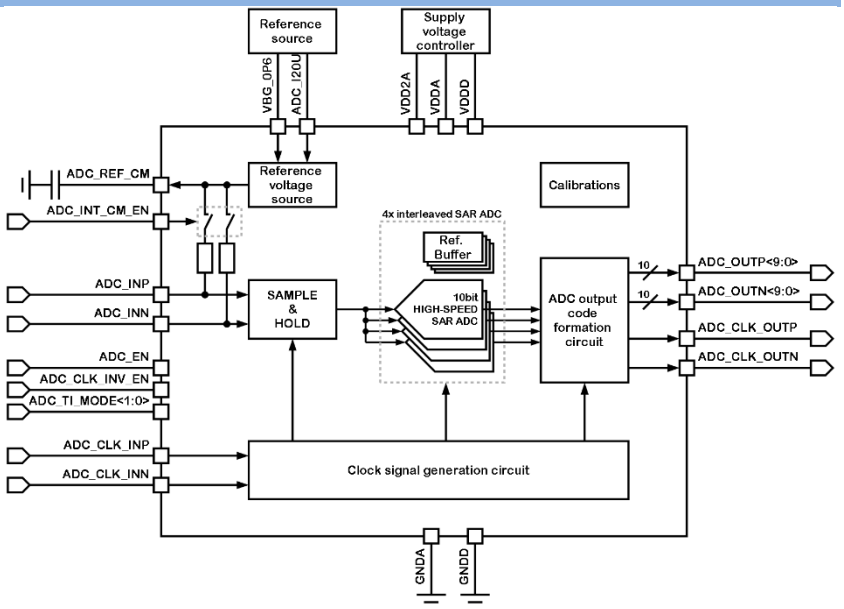
OVERVIEW

055TSMC_ADC_13 is a 10-bit 1-channel SAR ADC with sample rate from 10 to 150 MSPS that operates with 1V peak-to-peak input signal. The block consists of 4x interleaved SAR ADC core, sample-and-hold block, ADC output code formation circuit, clock signal generation circuit, reference voltage source and calibrations block. The ADC block has a separate power supply for the analog and digital parts of the circuit. The ADC settings allow you to put the block into standby mode.

IP technology: TSMC CMOS 55nm technology.

IP status: silicon proven.

Silicon area: 1.6mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	VDD2A		1.8	2.0	2.2	V
	VDDA	-	1.08	1.2	1.32	
	VDDD	-	1.08	1.2	1.32	
Operating temperature range	T_j	-	-40	+27	+85	°C
Current consumption	IDD	F_S = 50 MSPS	33	34	36	mA
		F_S = 100 MSPS	48	50	52	
		F_S = 125 MSPS	-	59	-	
		Standby mode	-	9.5	-	uA
Resolution	N	-	-	10	-	bit
Sampling rate	F_S	Minimal	-	10	-	MSPS
		Maximal	-	150	-	
Input voltage range	$V_{IN(p-p)}$	-	-	1	-	V
Input clock frequency	F_{CLK}	Minimal	-	10	-	MHz
		Maximal	-	150	-	
Spurious-free dynamic range	SFDR	@ F_S = 50 MHz and F_{IN} = 10.7 MHz	-	73.4	-	dB
Signal to noise ratio	SNR		-	55.5	-	dB
Effective number of bits	ENOB		-	8.9	-	bits
Input logic-high level	V_{IH}	For digital inputs	0.9*VDDD	-	VDDD	V
Input logic-low level	V_{IL}		0	-	0.1*VDDD	V