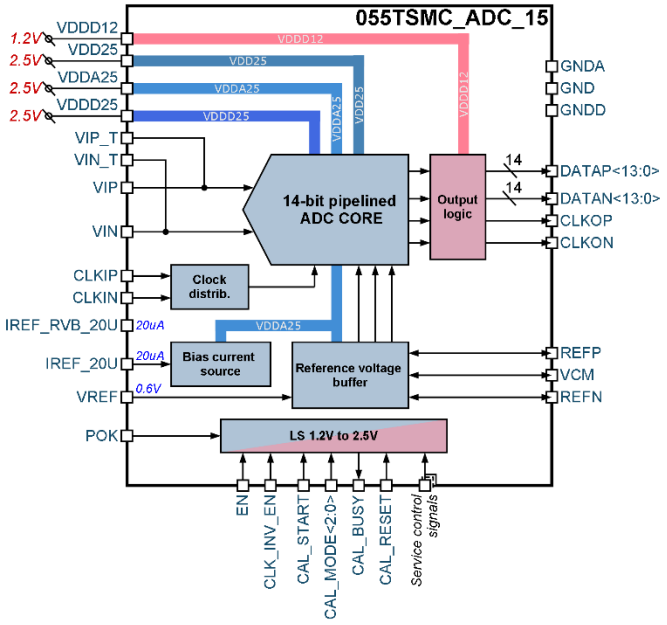
14-bit 1-channel 40 to 125 MSPS pipelined ADC

OVERVIEW

055TSMC_ADC_15 is a high-speed 14-bit ADC, employs a high-performance differential pipeline architecture. This ADC consist of 14-bit pipelined ADC core, output logic, reference voltage buffer, bias current source and clock distribution blocks. The ADC requires 2.5V analog supply, 1.2V and 2.5V digital supply, reference current 20uA and reference voltage 0.6V. ADC differential analog input voltage range from 1.0V to 3.1V. The ADC supports standby mode which allow to optimize power consumption for system need. There are two application options for the IP: internal reference voltage generator with external capacitor connection and capless solution; external reference voltage source.
IP technology: TSMC 55nm MS RF.
IP status: pre-silicon verification.
GDS area: 5.46mm^2.
Silicon area: 4.42mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{DD25}	-		2.375	2.5	2.625	V
	V_{DDA25}	-		2.375	2.5	2.625	V
Digital supply voltage	V_{DDD25}	-		2.375	2.5	2.625	V
	V_{DDD12}	-		1.14	1.2	1.26	V
Operating junction temperature range	T_j	-		-40	+27	+85	°C
Input capacitance	C_{IN}	-		-	4	-	pF
Reference voltage	V_{ref}	-		-	0.6	-	V
Reference current	I_{ref}	-		-	20	-	uA
Input clock frequency	F_{clk}	-		40	125	-	MHz
Sample rate	Fs	-		40	125	-	MSPS
Differential operating input range	A_{IN}	ADJ_REF<4:0> = (20)dec		-	2.0	-	V
Input common mode voltage	V_{CM}	SEL_VCM = (0)dec		-	$0.5V_{DDA25}$	-	V
Differential reference voltage	V_{REFP}	-		-	V_{CM}+0.5	-	V
	V_{REFN}	-		-	V_{CM}-0.5	-	V
Current consumption	I_{CC_VDD25}	T_j=-40÷100°C		-	32.8	39.2	mA
	I_{CC_VDDA25}	T_j=-40÷100°C		-	169.5	179.2	mA
	I_{CC_VDDD25}	T_j=-40÷100°C		-	29.5	35.7	mA
	I_{CC_VDDD12}	T_j=-40÷100°C		-	5.2	24	mA
Total power dissipation	P_{CN_TOTAL}	-		-	586	730	mW
Stand-by current	I_{STB}	-		-	5	37	uA
Spurious-free dynamic range	SFDR	Sin wave, T_j=-40÷100°C	F_{in}=10.01MHz	80	83.5	-	dB
			F_{in}=58.84MHz	76.8	81.9	-	dB
Signal-to-noise ratio	SNR	Sin wave, T_j=-40÷100°C	F_{in}=10.01MHz	69.2	73.9	-	dB
			F_{in}=58.84MHz	68.7	71.4	-	dB
ADC analog bandwidth	F_{BW3DB}	-		-	610	-	MHz
Latency	ΔT	-		-	45	-	clock cycles
Aperture delay	t_A	-		-	2.6	-	ns