14-bit 1-channel 40 to 160MSPS pipeline ADC

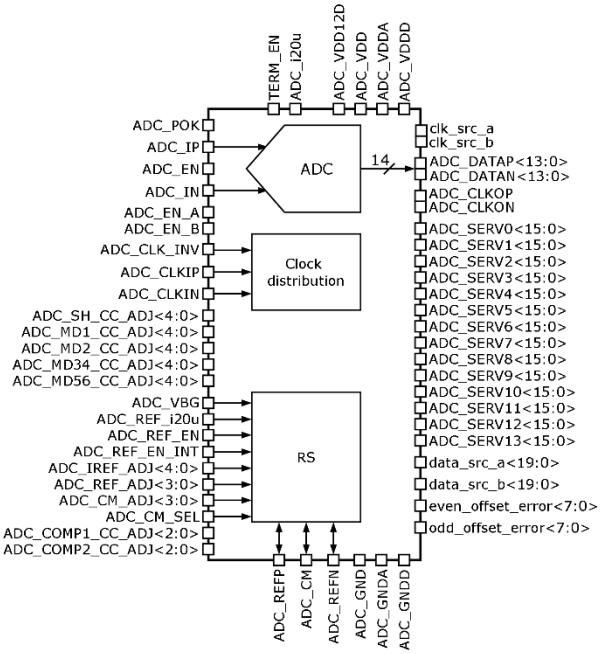
OVERVIEW

065STM_ADC_01 is a high-speed 1-channel 14-bit ADC based on a pipelined architecture. The ADC consists of three main blocks: the ADC, RS, and the clock signal distribution block. For the correct operation of the ADC, the following characteristics are required: analog power supply 2.375 ÷ 2.625V (**ADC_VDD**, **ADC_VDDA**), digital power supply 2.375 ÷ 2.625V (**ADC_VDDD**), digital power supply 1.08 ÷ 1.32V (**ADC_VDD12D**); two reference currents 20uA (**ADC_REF_i20u**, **ADC_i20u**); reference bandgap voltage for the RS block 1.2V; differential clock input with a duty cycle of 45 ÷ 55%. The block has sampling rate range of 40 to 160 MSPS, which is controlled by the input clock **ADC_CLKIP** and **ADC_CLKIN**.

IP technology: STM CMOS 65 nm.

IP status: silicon proven.

Area: 7.39mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{DDA}	-		2.375	2.5	2.625	V
	V_{DD}			2.375	2.5	2.625	
	V_{DDD}	-		2.375	2.5	2.625	
	V_{DD12D}	-		1.14	1.2	1.26	
Operating temperature range	T_j	-		-40	+25	+85	°C
Reference voltage	V_{bg}	-		-	1.2	-	V
Current consumption in active mode	I	F_S = 160MSPS		-	336	-	mA
Input reference current	I_{ref}	-		-	20	-	uA
Differential input voltage range	$A_{in\_p\text{-}p}$	-		-	2	-	V
Common mode voltage	V_{cm}	-		-	$0.5V_{DDA}$	-	V
Differential reference voltage	V_{refp}	-		-	V_{cm}+0.5	-	V
	V_{refn}	-		-	V_{cm}-0.5	-	
Clock input duty cycle	S	-		45	50	55	%
Bandwidth	BW	-		20	-	80	MHz
Resolution	N	-		-	14	-	bit
Clock frequency	F_{CLK}	-		40	-	160	MHz
Sampling rate	F_S	-		40	-	160	MSPS
Effective number of bits	ENOB	F_S = 40MSPS, F_{in_sin} = 10.7MHz		10.6	10.8	11.0	bit
		F_S = 160MSPS, F_{in_sin} = 21.4MHz		10.3	10.6	10.8	
Spurious free dynamic range	SFDR	F_S =40MSPS, F_{CLK} =80MHz	F_{in_sin} = 5MHz	79.2	83.3	88.3	dB
			F_{in_sin} = 10.7MHz	77.1	82.6	86.9	
			F_{in_sin} = 21.4MHz	74.2	79.2	83.5	
		F_S =80MSPS, F_{CLK} =160MHz	F_{in_sin} = 5MHz	77.9	83.0	88.9	
			F_{in_sin} = 10.7MHz	77.4	83.4	89.5	
			F_{in_sin} = 21.4MHz	78.3	82.7	88.8	
		F_S =160MSPS, F_{CLK} =160MHz	F_{in_sin} = 5MHz	73.0	78.4	85.3	
			F_{in_sin} = 10.7MHz	72.7	78.6	85.2	
			F_{in_sin} = 21.4MHz	73.1	78.2	83.8	
Signal-to-noise ratio	SNR	F_S =40MSPS, F_{CLK} =80MHz	F_{in_sin} = 5MHz	67.4	68.4	69.1	dB
			F_{in_sin} = 10.7MHz	67.5	68.0	68.8	
			F_{in_sin} = 21.4MHz	64.8	66.5	67.3	

Parameter	Symbol	Conditions		Value			Units
				min	typ.	max	
		F_S =80MSPS, F_{CLK} =160MHz	F_{in_sin} = 5MHz	66.8	67.8	68.6	
			F_{in_sin} = 10.7MHz	66.7	68.0	69.0	
			F_{in_sin} = 21.4MHz	66.3	67.5	68.4	
		F_S = 160MSPS, F_{CLK} =160MHz	F_{in_sin} = 5MHz	65.8	66.9	67.6	
			F_{in_sin} = 10.7MHz	65.8	67.0	67.8	
			F_{in_sin} = 21.4MHz	65.3	66.6	67.2	
Input high-logic level	V_{IH}	-		$0.9V_{DD12D}$	-	V_{DD12D}+0.3	V
Input low-logic level	V_{IL}	-		-0.3	-	+0.3	V
Output high-logic level	V_{OH}	-		V_{DD12D}-0.3	-	-	V
Output low-logic level	V_{OL}	-		-	-	0.4	V