10-bit up to 130 MSPS low-power high-speed pipeline ADC

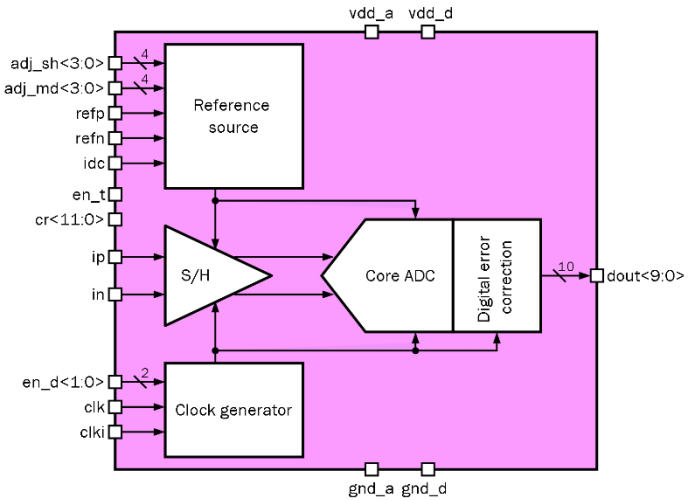
OVERVIEW

065TSMC_ADC_06 is 10-bit up to 130 MSPS low-power high-speed ADC which is based on pipelined architecture. ADC contains a five main blocks: sample and hold, core ADC, digital error correction, timing generation, reference voltage. The block requires: 1.08÷1.32 V analog supply, 1.08÷1.32 V digital supply; reference current 4.95÷5.05 uA; differential reference voltage 1.08÷1.32 V and 0 V; differential input clock with duty cycle 45÷55 %. ADC supports standby mode. There is also the ability to configure the operating modes of the ADC with digital registers: register **en_d<1:0>** controls the differential input clock, register **cr<11:0>** controls the modes of the core ADC, register **adj_sh<3:0>** adjusts current of the sample and hold, register **adj_md<3:0>** adjusts current of the core ADC.

IP technology: TSMC CMOS LP 65 nm.

IP status: silicon proven.

Area: 0.28mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Operating temperature range	T_j	-	-40	+27	+125	°C
Analog blocks supply voltage	V_{dd_a}	-	1.08	1.2	1.32	V
Digital blocks supply voltage	V_{dd_d}	-	1.08	1.2	1.32	V
Differential reference voltage	V_{refp}	-	1.08	1.2	1.32	V
	V_{refn}	-	-	0	-	V
Reference current	I_{ref}	-	4.95	5	5.05	uA
Duty cycle	S	-	45	50	55	%
Resolution	N	-	-	10	-	bit
Sampling rate	F_s	-	-	-	130	MSPS
Power dissipation	P_{dd}	F_s= 130 MSPS	-	34	-	mW
		F_s = 80 MSPS	-	25	-	mW
		F_s = 50 MSPS	-	21	-	mW
Current consumption	I_{cc}	F_s = 130 MSPS	-	28	-	mA
		F_s = 80 MSPS	-	20	-	mA
		F_s = 50 MSPS	-	17	-	mA
Standby current	I_{stb}	-	-	10	-	uA
Differential input voltage range peak-to-peak	$A_{IN\ p\text{-}p}$	-	-	1.2	-	V
Input common mode voltage	U	-	-	0.6	-	V
Full power bandwidth	F_B	F_s = 130 MSPS	-	260	-	MHz
		F_s = 80 MSPS	-	160	-	MHz
		F_s = 50 MSPS	-	100	-	MHz
Spurious-free dynamic range	SFDR	F_s = 50 - 130 MSPS, Fin = 3 - 8.125 MHz	-	68	-	dB
Signal-to-noise ratio	SNR	F_s = 50 - 130 MSPS, Fin = 3 - 8.125 MHz	-	60	-	dB
Signal-to-noise and distortion ratio	SINAD	F_s = 80 - 130 MSPS, Fin = 5 - 8.125 MHz	-	59	-	dB
		F_s = 50 MSPS, Fin = 3.125 MHz	-	60	-	dB
Effective number of bits	ENOB	F_s = 130 MSPS	-	9.1	-	bit
		F_s = 80 MSPS, F_s = 50 MSPS	-	9.3	-	bit
Differential nonlinearity	DNL	F_s = 80 MSPS	-	±0.5	-	LSB
Integral nonlinearity	INL	F_s = 80 MSPS	-	±1	-	LSB
Input high-logic level	V_{IH}	For digital inputs	0.7 V_{dd_d}	-	-	V
Input low-logic level	V_{IL}		-	-	0.3 V_{dd_d}	V