10-bit 1-channel 50/100 MSPS ADC

SPECIFICATION

1. FEATURES

- TSMC CMOS 65 nm
- Resolution 10 bit
- 1 channel
- Different power supplies for digital (1.2 V) and analog parts (1.2 V)
- Sampling rate up to 100 MSPS
- Stand-by mode (current consumption 10 uA)
- Low-power dissipation:
  34 mW at 100 MSPS
  21 mW at 50 MSPS
- Differential full-scale input range peak-to-peak 1 V
- Dynamic performance:
  66.0 dB SFDR, 54.2 dB SINAD at 50 MSPS and fin = 10.7 MHz
  66.3 dB SFDR, 53.0 dB SINAD at 100 MSPS and fin = 10.7 MHz
- Differential nonlinearity ±0.79 LSB
- Integral nonlinearity ±0.94 LSB
- Compact die area 0.26 mm^2
- Portable to other technologies (upon request)

2. APPLICATION

- WiFi, WiMax
- Mobile Communications
- High quality imaging video systems
- Data acquisition systems
- Portable ultrasound and digital beam-forming systems

3. OVERVIEW

The 10-bit 50/100 MSPS ADC employs a high-performance front-end sample-and-hold with differential multistage pipelined architecture and output error correction logic. The biasing circuit and the clock generator are also included to provide a complete ADC. The ADC operates with sampling rate up to 100 MSPS and a corresponding input clock up to 200 MHz (input clock is divided by two). The ADC can be configured to achieve addition power saving at low sampling rate, supports stand-by mode and features the excellent dynamic and static performance, wide bandwidth inputs, low power consumption and compact die area.
The block is designed on TSMC CMOS 65 nm technology.

4. STRUCTURE

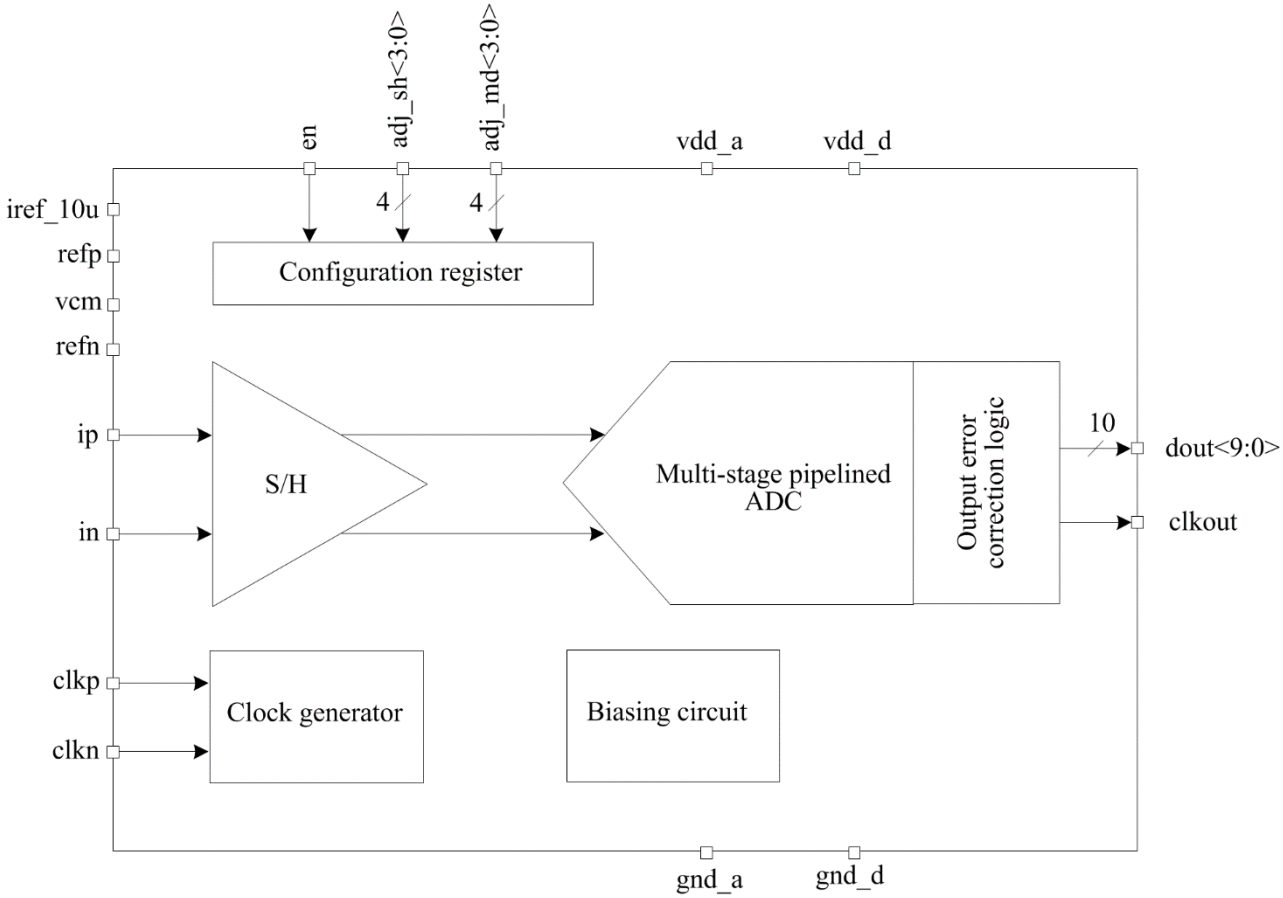

Figure 1: 10-bit 50/100 MSPS ADC structure

5. PIN DESCRIPTION

Name	Direction	Description
iref_10u	I	Reference current (10 uA)
ip in	I	Analog differential input (1 V peak-to-peak)
clkp clkn	I	200 MHz differential clock input
refp	I	Positive reference voltage (0.8 V)
vcm	I	Common mode voltage (0.55 V)
refn	I	Negative reference voltage (0.3 V)
en	I	ADC enable: “0” disabled “1” enabled
adj_sh<3:0>	I	Register of adjust reference current the sample and hold: “0000” unused “0001” 5 uA … with step of 5 uA “1111” 75 uA
adj_md<3:0>	I	Register of adjust reference current the multi-stage ADC: “0000” unused “0001” 5 uA … with step of 5 uA “1111” 75 uA
dout<9:0>	O	Output data
clkout	O	100 MHz output clock
vdd_a	I/O	Analog block supply voltage (1.2 V)
vdd_d	I/O	Digital blocks supply voltage (1.2 V)
gnd_a	I/O	Analog blocks ground
gnd_d	I/O	Digital blocks ground

6. FUNTIONAL DESCRIPTION

The input clock is divided by two and after t_{d1} time analog input voltage is sampled by the positive edge. The output data after the conversion latency of 8 clock cycles is latched.

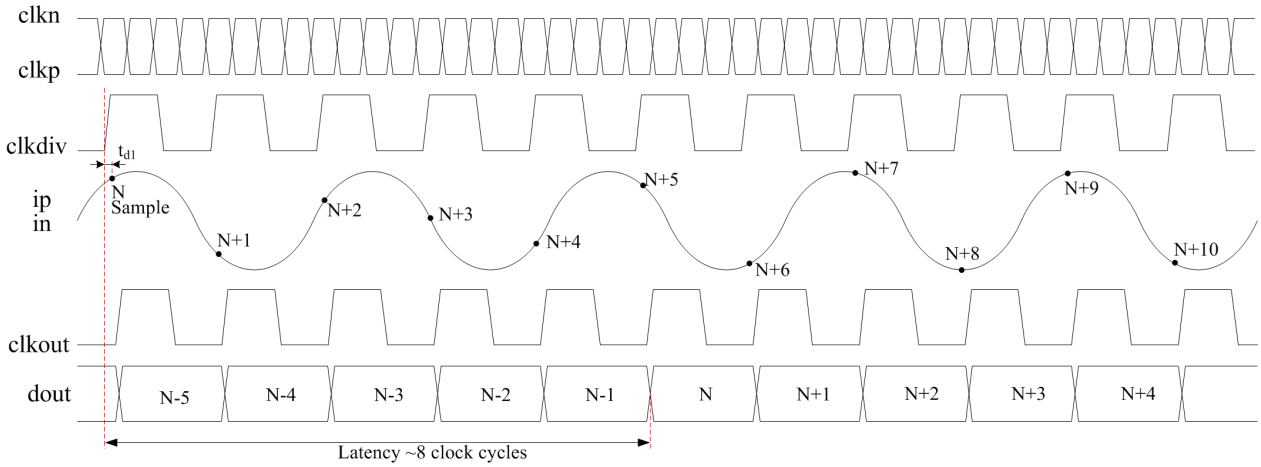

Figure 2: Timing diagram for normal operation

7. CURRENT CONSUMPTION PROGRAMMABILITY

There is also ability to adjust reference current the sample-and-hold and multi-stage pipeline ADC. The values of reference current determine current consumption. Adjustable reference current allows configuring operation mode related to static, dynamic performance and sampling rate.

$$I_{DC} = 5\ \text{uA} \cdot 440 \cdot \text{adj\_sh} + 5\ \text{uA} \cdot 440 \cdot \text{adj\_md},$$

where adj_sh – decimal representation register of adjust reference current the sample and hold; adj_md – decimal representation register of adjust reference current the multi-stage pipeline ADC.

8. LAYOUT DESRIPTION

8.1 TECHNOLOGY OPTIONS

ADC is designed under TSMC 65 nm LP CMOS technology process with following options:

- 4x1z1u metal option
- 1.2 V standard Vt MOS
- 1.2 V low Vt MOS
- 2.0 fF/um^2 MIM capacitor
- P+polysilicon OP resistor

8.2 PHYSICAL DIMENTIONS

ADC layout dimensions are given in the table 1.

Table 1: Block dimension.

Dimension	Value	Unit
Height	410	um
Width	630	um

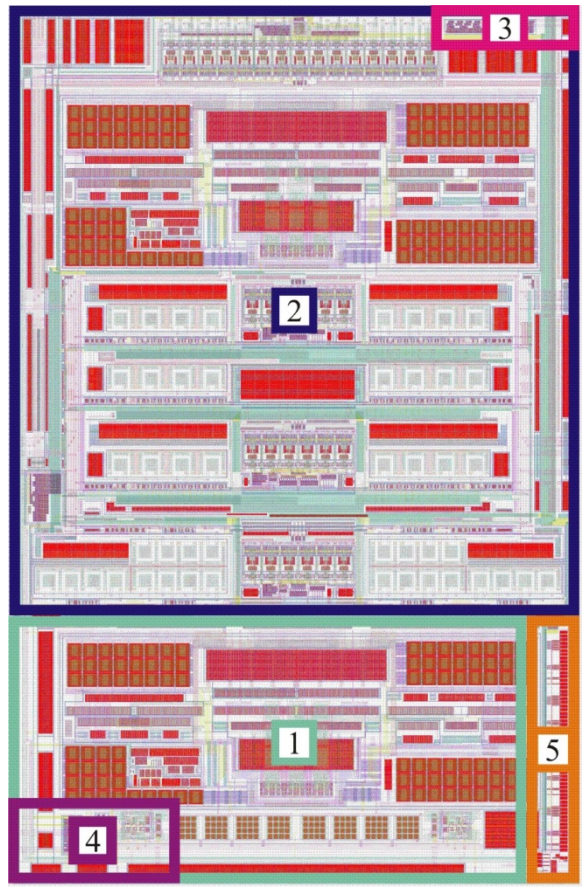

Figure 3: ADC layout

1. Sample and hold
2. Multistage ADC
3. Output error correction logic
4. Clock generator
5. Biasing circuit

9. INTEGRATION GUIDELINES

9.1 PLACE AND ROUTE GUIDELINES

1) ADC analog inputs ip and in signals should be connected to analog IO PADs or an internal analog circuits (intermediate frequency amplifier, filter). IO PADs should not have an internal resistor to increase bandwidth.
2) Wiring of analog inputs should be symmetrical and as short as possible.
3) Noisy, power and high-frequency circuits should not place near ADC.
4) Minimum space 40 um between ADC and other circuits should be kept.
5) Minimum metal wiring width is 50 um for vdd_a and gnd_a. Multiple layers of metal can be used to reduce layout space.
6) Minimum metal wiring width is 10 um for vdd_d and gnd_d. Multiple layers of metal can be used to reduce layout space.
7) Allowable total resistance of vdd_a and gnd_a are 0.5 Ohm. Blocking capacitors should be added and placed as close as possible.
8) Allowable total resistance of vdd_a and gnd_a are 2 Ohm. Blocking capacitors should be added and placed as close as possible.

10. OPERATING CHARACTERISTICS

10.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status silicon proven
Area 0.26 mm^2

10.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a}=1.14÷1.26 V, V_{dd_d}=1.14÷1.26 V and T_j =-40÷+85°C, typical values are at V_{dd_a} = 1.2 V, V_{dd_d}=1.2 V, T_j = +27°C, unless otherwise noted.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Operating temperature range	T_j	-	-40	27	+85	°C
Power Supply Requirements						
Analog supply voltage	V_{dd_a}	-	1.14	1.2	1.26	V
Digital supply voltage	V_{dd_d}	-	1.14	1.2	1.26	V
Current consumption in normal mode	I_{cn}	F_S= 50 MSPS	-	17	-	mA
		F_S= 100 MSPS	-	28	-	mA
Current consumption in stand-by mode	I_s	-	-	10	-	uA
Power consumption in normal mode	P_{cn}	F_S= 50 MSPS	-	21	-	mW
		F_S= 100 MSPS	-	34	-	mW
DC Accuracy						
Resolution	N	-	-	10	-	bit
Differential nonlinearity	DNL	F_S= 50 MSPS	-	±0.79	-	LSB
Integral nonlinearity	INL	F_S= 50 MSPS	-	±0.94	-	LSB
Offset error	OE	F_S= 50 MSPS	-	±2.0	-	LSB
Gain error	GE	F_S= 50 MSPS	-	±0.11	-	LSB
Analog Inputs						
Differential full-scale input range	$A_{IN\ p\text{-}p}$	-	-	1	-	V
Input common-mode voltage	V_{cm_in}	-	0.5	-	0.55	V
Input capacitance	C_{eff_in}	-	-	4	-	pF
Input resistance	R_{eff_in}	-	-	100	-	kOhm
Digital Inputs and Outputs						
Output logic coding	-	-	Offset binary			code
Input logic-level high	V_{IH}	-	0.7 V_{dd_d}	-	-	V
Input logic-level low	V_{IL}	-	-	-	0.3 V_{dd_d}	V
Timing Information						
Input clock	F_{clk}	-	-	-	200	MHz
Sampling rate	F_s	F_{clk}/2	10	-	100	MSPS
Duty cycle	S	-	45	50	55	%
Latency	L	-	-	8	-	clock cycles
External Reference Requirements						
Reference current	I_{ref}	-	9.9	10	10.1	uA
Positive reference voltage	V_{refp}	-	-	0.80	-	V
Common mode voltage	V_{cm}	-	-	0.55	-	V
Negative reference voltage	V_{refn}	-	-	0.30	-	V

Table “Electrical characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Dynamic characteristic at F_S= 50 MSPS						
Input frequency range	fin	-	0	-	530	MHz
Signal-to-noise ratio	SNR	fin = 10.7 MHz	-	54.3	-	dB
		fin = 21.4 MHz	-	53.5	-	
		fin = 30 MHz	-	53.0	-	
		fin = 70 MHz	-	49.8	-	
Signal-to-noise and distortion ratio	SINAD	fin = 10.7 MHz	-	54.2	-	dB
		fin = 21.4 MHz	-	53.4	-	
		fin = 30 MHz	-	52.9	-	
		fin = 70 MHz	-	49.6	-	
Effective number of bits	ENOB	fin = 10.7 MHz	-	8.7	-	bits
		fin = 21.4 MHz	-	8.6	-	
		fin = 30 MHz	-	8.5	-	
		fin = 70 MHz	-	8.0	-	
Worst second or third harmonic	-	fin = 10.7 MHz	-	78	-	dB
		fin = 21.4 MHz	-	81	-	
		fin = 30 MHz	-	67	-	
		fin = 70 MHz	-	76	-	
Spurious-free dynamic range	SFDR	fin = 10.7 MHz (see Fig. 18)	-	64	-	dB
		fin = 21.4 MHz (see Fig. 20)	-	61	-	
		fin = 30 MHz (see Fig. 22)	-	58	-	
		fin = 70 MHz	-	54.5	-	
Two-tone spurious-free-dynamic range	Two-tone SFDR	fin = 10.7 MHz	-	64	-	dB
		fin = 21.4 MHz	-	61	-	
		fin = 30 MHz	-	58	-	
Intermodulation distortion third-order	IMD3	fin = 10.7 MHz (see Fig. 19)	-	74	-	dB
		fin = 21.4 MHz (see Fig. 21)	-	76	-	
		fin = 30 MHz (see Fig. 23)	-	71	-	
Full power bandwidth	F_B	-	-	560	-	MHz
Dynamic characteristic at F_S= 100 MSPS						
Input frequency range	fin	-	0	-	530	MHz
Signal-to-noise ratio	SNR	fin = 10.7 MHz	-	53.1	-	dB
		fin = 21.4 MHz	-	52.4	-	
		fin = 30 MHz	-	52.0	-	
		fin = 70 MHz	-	48.7	-	
Signal-to-noise and distortion ratio	SINAD	fin = 10.7 MHz	-	53.0	-	dB
		fin = 21.4 MHz	-	52.2	-	
		fin = 30 MHz	-	51.8	-	
		fin = 70 MHz	-	48.5	-	
Effective number of bits	ENOB	fin = 10.7 MHz	-	8.5	-	bit
		fin = 21.4 MHz	-	8.4	-	
		fin = 30 MHz	-	8.3	-	
		fin = 70 MHz	-	7.8	-	
Worst second or third harmonic	-	fin = 10.7 MHz	-	72	-	dB
		fin = 21.4 MHz	-	67	-	
		fin = 30 MHz	-	67	-	
		fin = 70 MHz	-	59	-	
Spurious-free dynamic range	SFDR	fin = 10.7 MHz	-	66.3	-	dB
		fin = 21.4 MHz	-	63.7	-	
		fin = 30 MHz	-	60.5	-	
		fin = 70 MHz	-	52.1	-	
Full power bandwidth	F_B	-	-	400	-	MHz

11. TYPICAL CHARACTERISTICS

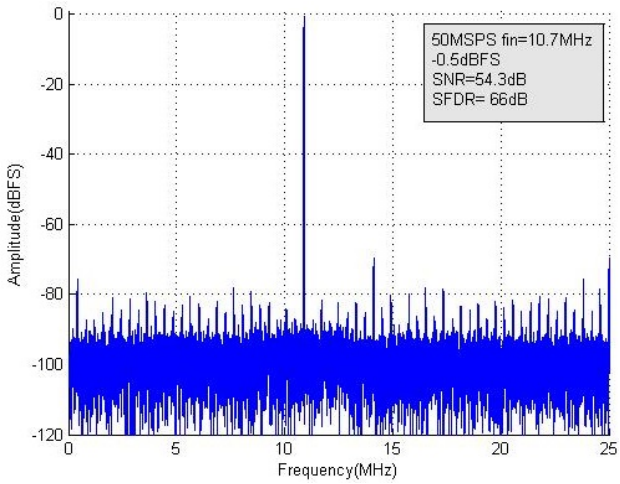

Figure 4: Spectrum with F_S= 50 MSPS and fin= 10.7 MHz

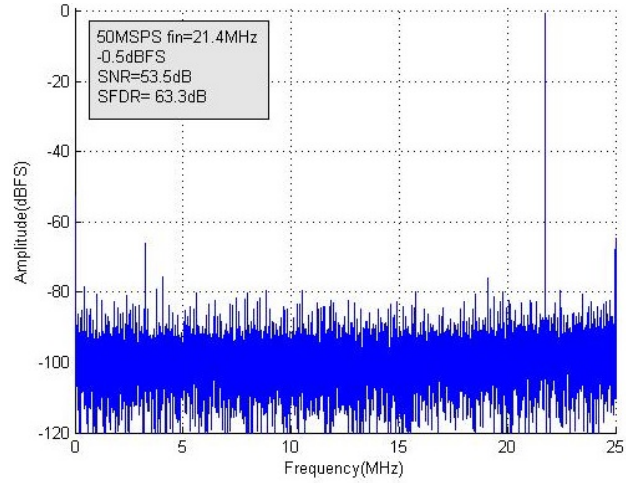

Figure 5: Spectrum with F_S= 50 MSPS and fin= 21.4 MHz

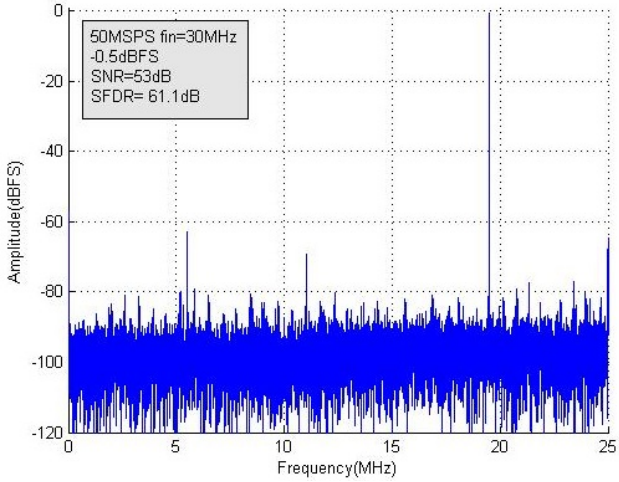

Figure 6: Spectrum with F_S= 50 MSPS and fin= 30 MHz

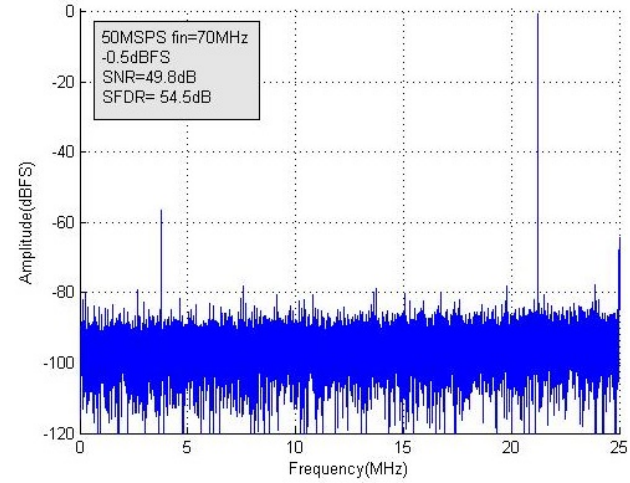

Figure 7: Spectrum with F_S= 50 MSPS and fin= 70 MHz

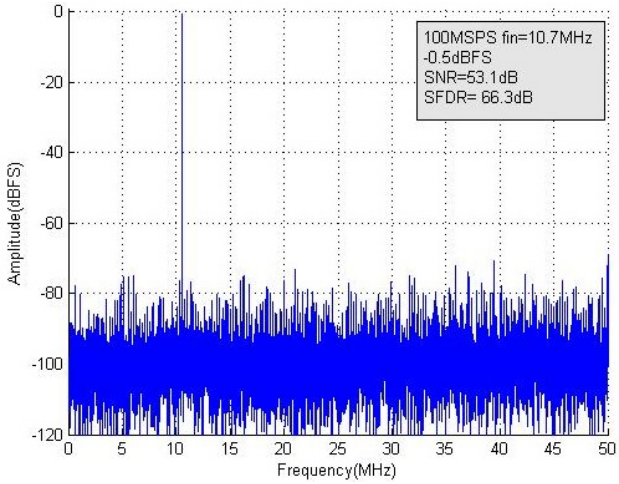

Figure 8: Spectrum with F_S= 100 MSPS and fin= 10.7 MHz

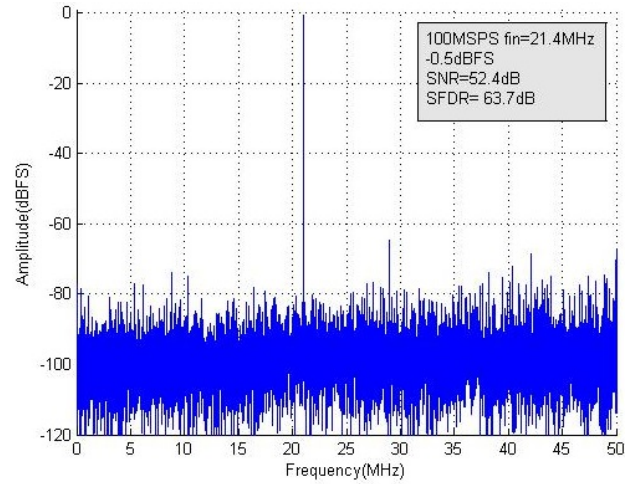

Figure 9: Spectrum with F_S= 100 MSPS and fin= 21.4 MHz

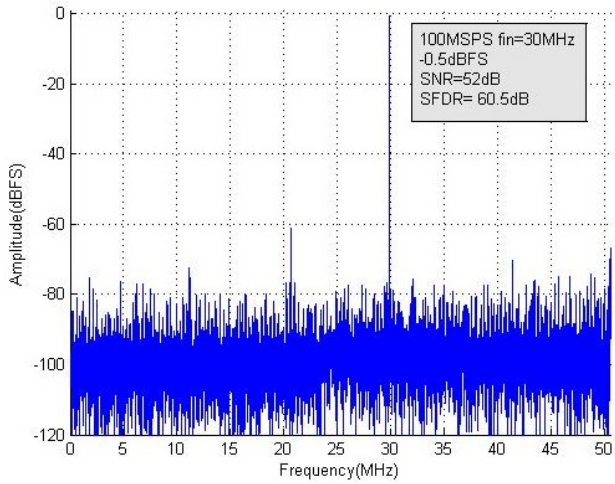

Figure 10: Spectrum with F_S= 100 MSPS and fin= 30 MHz

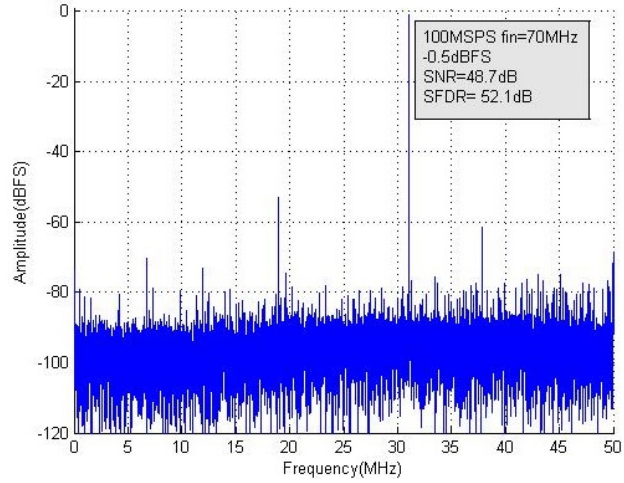

Figure 11: Spectrum with F_S= 100 MSPS and fin= 70 MHz

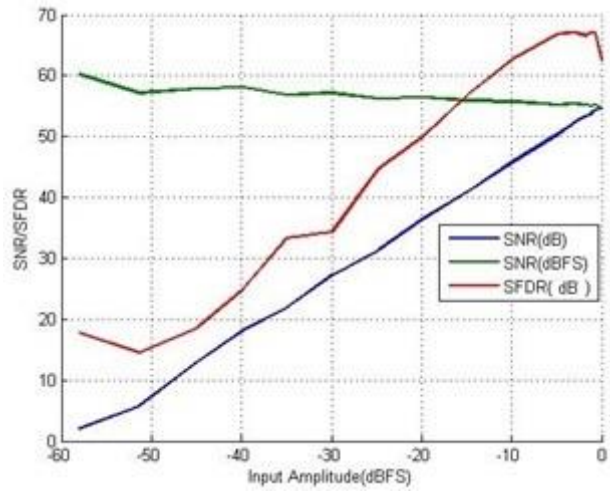

Figure 12: SNR/SFDR vs. input amplitude with F_S= 50 MSPS and fin= 10.7 MHz

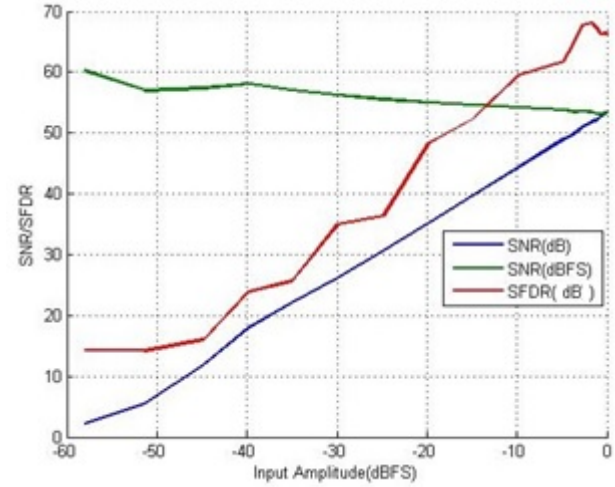

Figure 13: SNR/SFDR vs. input amplitude with F_S= 100 MSPS and fin= 10.7 MHz

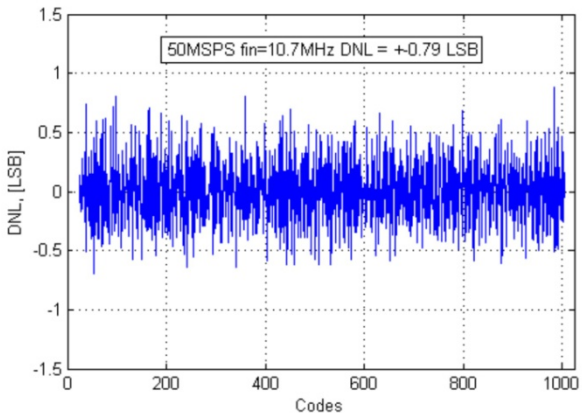

Figure 14: DNL with F_S= 50 MSPS and fin= 10.7 MHz

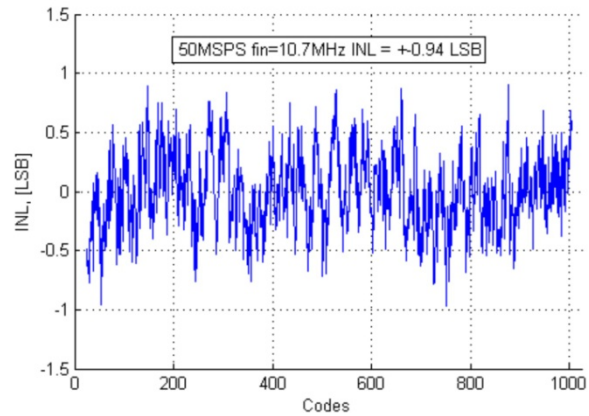

Figure 15: INL with F_S= 50 MSPS and fin= 10.7 MHz

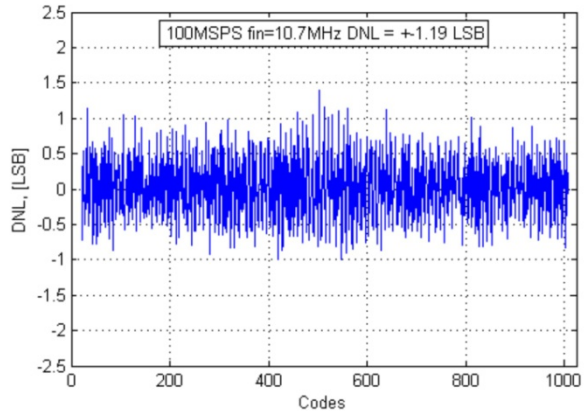

Figure 16: DNL with F_S= 100 MSPS and fin= 10.7 MHz

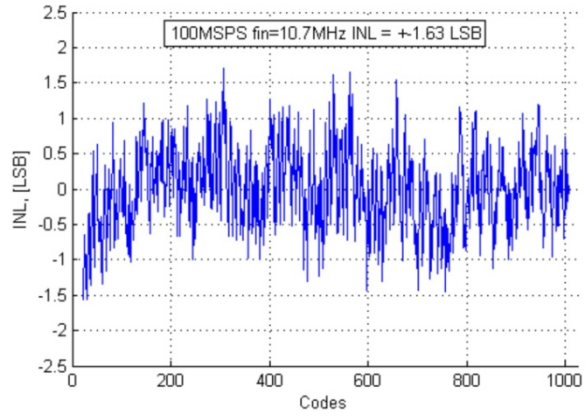

Figure 17: INL with F_S= 100 MSPS and fin= 10.7 MHz

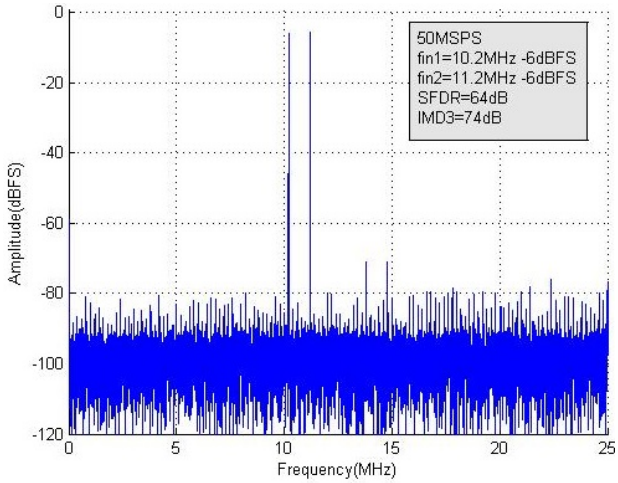

Figure 18: Spectrum with F_S= 50 MSPS, fin1= 10.2 MHz and fin2= 11.2 MHz

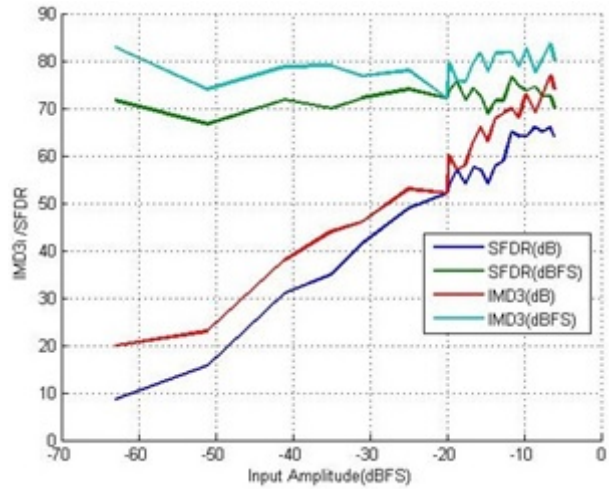

Figure 19: IMD3/SFDR vs. input amplitude with F_S= 50 MSPS, fin1= 10.2 MHz and fin2= 11.2 MHz

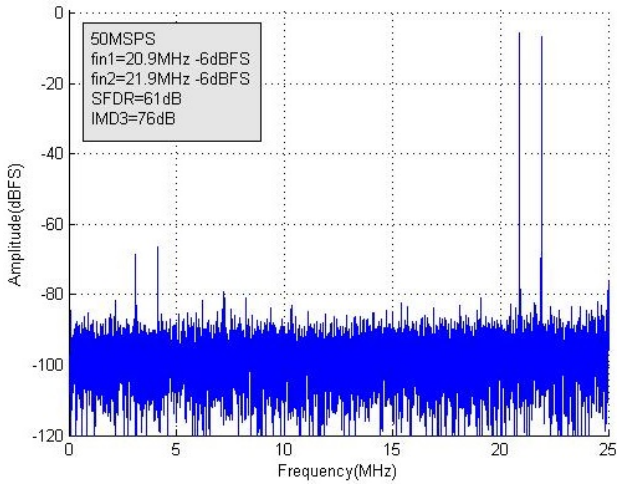

Figure 20: Spectrum with F_S= 50 MSPS, fin1= 20.9 MHz and fin2= 21.9 MHz

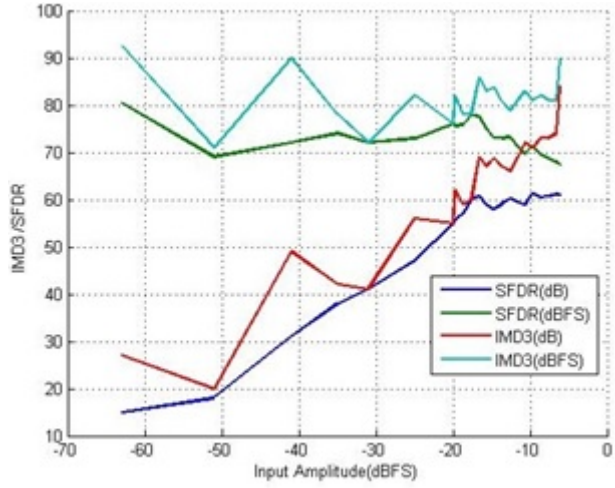

Figure 21: IMD3/SFDR vs. input amplitude with F_S= 50 MSPS, fin1= 20.9 MHz and fin2= 21.9 MHz

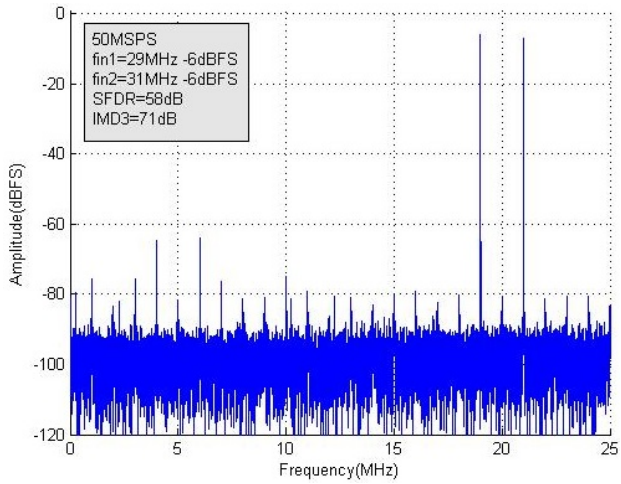

Figure 22: Spectrum with F_S= 50 MSPS, fin1= 29 MHz and fin2= 31 MHz

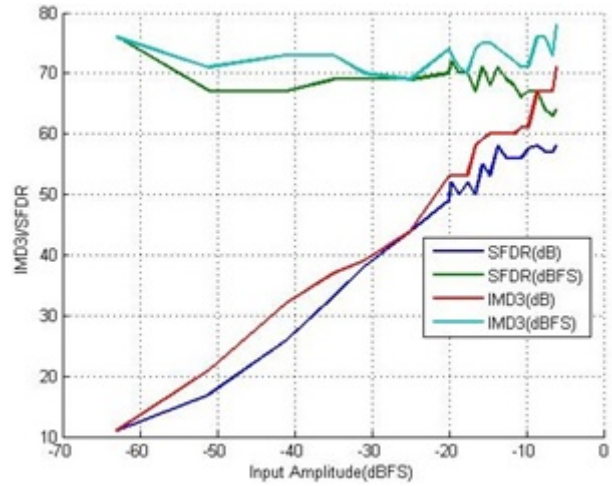

Figure 23: IMD3/SFDR vs. input amplitude with F_S= 50 MSPS, fin1= 29 MHz and fin2= 31 MHz

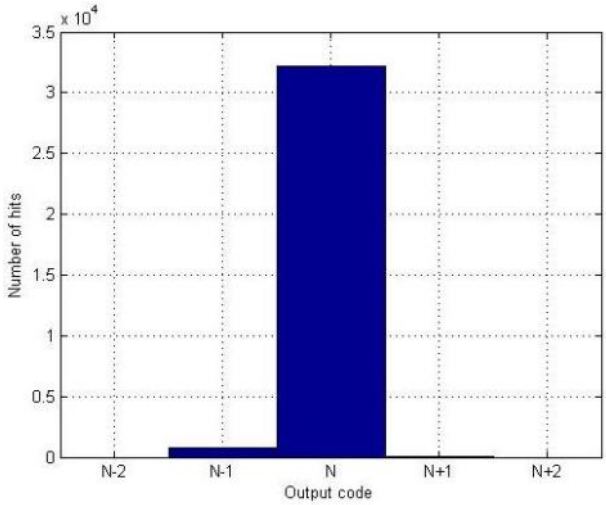

Figure 24: Input histogram F_S= 50 MSPS

12. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section 3 was changed (refer to page 1)
   - Section 4 was changed (refer to page 2)
   - Section 5 was changed (refer to page 3)
   - Subsection 10.2 was changed (refer to page 5)
2. From version 1.1:
   - Section 1 was changed (refer to page 1)
   - Section 3 was changed (refer to page 1)
   - Section 4 was changed (refer to page 2)
   - Section 5 was changed (refer to page 3)
   - Section 6 shifted to section 8
   - Section 6 was added (refer to page 4)
   - Section 7 shifted to section 9
   - Section 7 was added (refer to page 4)
   - Section 8 was changed (refer to page 4)
   - Section 9 shifted to section 10
   - Section 9 was added (refer to page 6)
   - Subection 10.2 was changed (refer to page 7)