10-bit 1-channel 50/100 MSPS pipeline ADC

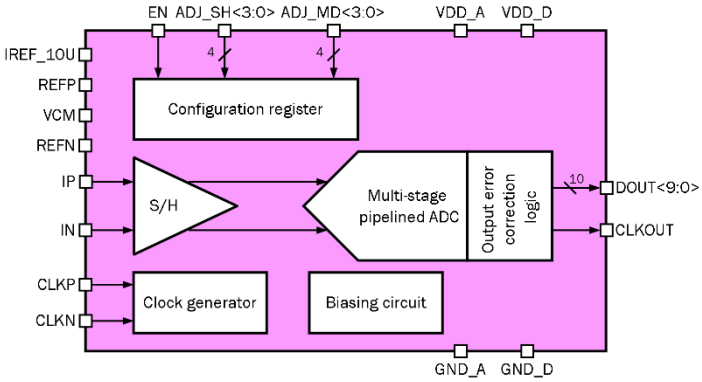
OVERVIEW

065TSMC_ADC_08 employs a high-performance front-end sample-and-hold with differential multistage pipelined architecture and output error correction logic. The biasing circuit and the clock generator are also included to provide a complete ADC. The ADC operates with sampling rate up to 100 MSPS and a corresponding input clock up to 200 MHz (input clock is divided by two). The ADC can be configured to achieve addition power saving at low sampling rate, supports stand-by mode and features the excellent dynamic and static performance, wide bandwidth inputs, low power consumption and compact die area.

IP technology: TSMC CMOS 65 nm.

IP status: silicon proven.

Area: 0.26mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{DD_A}	-		1.14	1.2	1.26	V
Digital supply voltage	V_{DD_D}	-		1.14	1.2	1.26	V
Operating temperature range	T_j	-		-40	+27	+85	°C
Current consumption in normal mode	I_{CC}	F_S = 50 MSPS		-	17	-	mA
		F_S = 100 MSPS		-	28	-	mA
Current consumption in stand-by mode	I_{STB}	-		-	10	-	uA
Power consumption in normal mode	P_C	F_S = 50 MSPS		-	21	-	mW
		F_S = 100 MSPS		-	34	-	mW
Reference current	I_{REF}	-		9.9	10	10.1	uA
Positive reference voltage	V_{REFP}	-		-	0.80	-	V
Negative reference voltage	V_{REFN}	-		-	0.30	-	V
Resolution	N	-		-	10	-	bit
Differential nonlinearity	DNL	F_S = 50 MSPS		-	±0.79	-	LSB
Integral nonlinearity	INL	F_S = 50 MSPS		-	±0.94	-	LSB
Input clock	F_{CLK}	-		-	-	200	MHz
Sampling rate	F_S	@F_{CLK}/2		10	-	100	MSPS
Common mode voltage	V_{CM}	-		-	0.55	-	V
Signal-to-noise and distortion ratio	SINAD	F_S=50 MSPS	F_{IN} = 10.7 MHz	-	54.2	-	dB
			F_{IN} = 21.4 MHz	-	53.4	-	
			F_{IN} = 30 MHz	-	52.9	-	
			F_{IN} = 70 MHz	-	49.6	-	
		F_S=100 MSPS	F_{IN} = 10.7 MHz	-	53.0	-	dB
			F_{IN} = 21.4 MHz	-	52.2	-	
			F_{IN} = 30 MHz	-	51.8	-	
			F_{IN} = 70 MHz	-	48.5	-	
Spurious-free dynamic range	SFDR	F_S=50 MSPS	F_{IN} = 10.7 MHz	-	64	-	dB
			F_{IN} = 21.4 MHz	-	61	-	
			F_{IN} = 30 MHz	-	58	-	
			F_{IN} = 70 MHz	-	54.5	-	
		F_S=100 MSPS	F_{IN} = 10.7 MHz	-	66.3	-	dB
			F_{IN} = 21.4 MHz	-	63.7	-	
			F_{IN} = 30 MHz	-	60.5	-	
			F_{IN} = 70 MHz	-	52.1	-	
Input logic-level high	V_{IH}	-		0.7 V_{DD_D}	-	V_{DD_D}	V
Input logic-level low	V_{IL}	-		0	-	0.3 V_{DD_D}	V