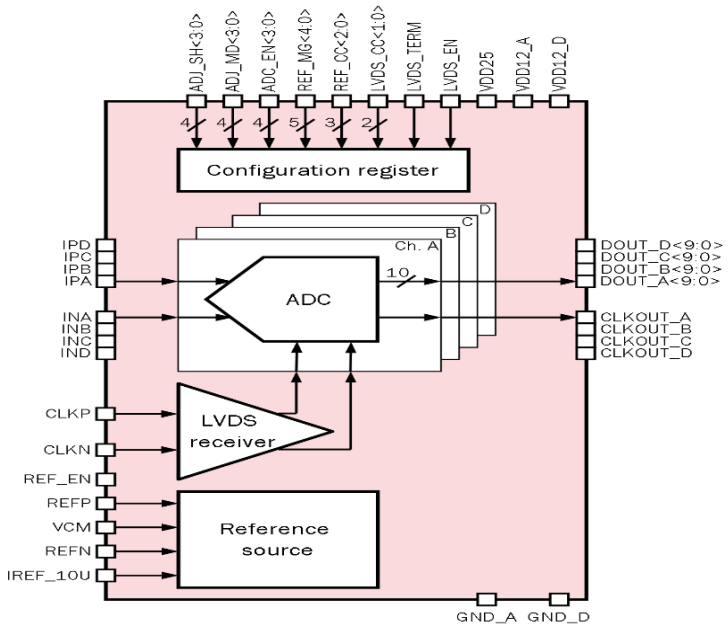
10-bit 4-channel 5-100 MSPS pipeline ADC

OVERVIEW

065TSMC_ADC_09 employs a high-performance front-end sample-and-hold with differential multistage pipelined architecture and output error correction logic. The reference generator, current source and LVDS receiver are also included to provide a complete ADC. The ADC operates with sampling rate up to 100 MSPS and a corresponding input clock up to 200 MHz (input clock is divided by two). The ADC can be configured to achieve addition power saving at low sampling rate, supports standby mode and features the excellent dynamic and static performance, wide bandwidth inputs, low power consumption and compact die area.
IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 1.32mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Operating temperature range	T_j	-		-40	27	+85	°C
Analog supply voltage	V_{dd12_a}	-		1.14	1.2	1.26	V
	V_{dd25}	-		2.25	2.5	2.75	V
Digital supply voltage	V_{dd12_d}	-		1.14	1.2	1.26	V
Current consumption in normal mode	I_{cn}	F_s = 50 MSPS		-	80	-	mA
		F_s = 100 MSPS		-	123	-	mA
Current consumption in standby mode	I_s	-		-	50	-	uA
Power consumption in normal mode	P_{cn}	F_s = 50 MSPS		-	96	-	mW
		F_s = 100 MSPS		-	147	-	mW
Current consumption in normal mode	I_{cn}	F_s = 50 MSPS		-	80	-	mA
Resolution	N	-		-	10	-	bit
Differential nonlinearity	DNL	F_s = 50 MSPS		-	±0.79	-	LSB
Integral nonlinearity	INL	F_s = 50 MSPS		-	±0.94	-	LSB
Offset error	OE	F_s = 50 MSPS		-	±2.0	-	LSB
Gain error	GE	F_s = 50 MSPS		-	±0.11	-	LSB
Input clock	F_{clk}	-		10	-	200	MHz
Sampling rate	F_s	F_{clk}/2		5	-	100	MSPS
Reference current	I_{ref}	-		9.9	10	10.1	uA
Positive reference voltage	V_{refp}	-		-	0.80	-	V
Common mode voltage	V_{cm}	-		-	0.55	-	V
Negative reference voltage	V_{refn}	-		-	0.30	-	V
Signal-to-noise ratio	SNR	F_s= 50 MSPS	F_{in} = 10.7 MHz	-	54.3	-	dB
			F_{in} = 30 MHz	-	53.0	-	dB
		F_s= 100 MSPS	F_{in} = 10.7 MHz	-	53.1	-	dB
			F_{in} = 30 MHz	-	52.0	-	dB
Spurious-free dynamic range	SFDR	F_s= 50 MSPS	F_{in} = 10.7 MHz	-	66.0	-	dB
			F_{in} = 30 MHz	-	61.1	-	dB
		F_s= 100 MSPS	F_{in} = 10.7 MHz	-	66.3	-	dB
			F_{in} = 30 MHz	-	60.5	-	dB
Full power bandwidth	F_B	@50 MSPS/ @100 MSPS		-	560/400	-	MHz
Input high-logic level	V_{IH}	-		$0.7V_{dd12\_d}$	-	V_{dd12_d}	V
Input low-logic level	V_{IL}	-		0	-	$0.3V_{dd12\_d}$	V