
12-bit 50/100/125 MSPS 4-channel ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- High speed pipelined ADC
- Resolution 12 bit
- Conversion rate 50/100/125 MHz
- Different power supplies for digital (1.2 V) and analog (1.2 V) parts
- Low standby current 40 uA
- Low power dissipation:
 - 178 mW at 50 MSPS
 - 256 mW at 100 MSPS
 - 298 mW at 125 MSPS
- Total harmonic distortion (THD):
 - 77.4 dB at 50 MSPS and $F_{IN} = 10.7$ MHz
 - 74.7 dB at 100 MSPS and $F_{IN} = 10.7$ MHz
 - 68.5 dB at 125 MSPS and $F_{IN} = 21.4$ MHz
- Spurious-free dynamic range (SFDR):
 - 73.7 dB at 50 MSPS and $F_{IN} = 10.7$ MHz
 - 73.4 dB at 100 MSPS and $F_{IN} = 10.7$ MHz
 - 70.8 dB at 125 MSPS and $F_{IN} = 21.4$ MHz
- Signal-to-noise ratio (SNR):
 - 59.3 dB at 50 MSPS and $F_{IN} = 10.7$ MHz
 - 59.3 dB at 100 MSPS and $F_{IN} = 10.7$ MHz
 - 58.1 dB at 125 MSPS and $F_{IN} = 21.4$ MHz
- Compact die area 4.58 mm²
- Portable to other technologies (upon request)

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- High quality imaging video systems
- WiFi, WiMax
- Mobile Communications
- High quality imaging video systems
- Data acquisition systems

3 OVERVIEW

The low-power high-speed 12-bit ADC employs a high-performance differential pipeline architecture. The ADC consists of LVDS receiver, reference currents circuit, reference voltage circuit and 4 channels, which contain a core ADC and output logic. The ADC requires: $1.08 \div 1.32$ V analog supply, $1.08 \div 1.32$ V digital supply, reference current $9.9 \div 10.1$ uA and differential input clock. The ADC supports standby mode which does possible state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.

The block is designed on TSMC CMOS 65 nm technology.

4 STRUCTURE

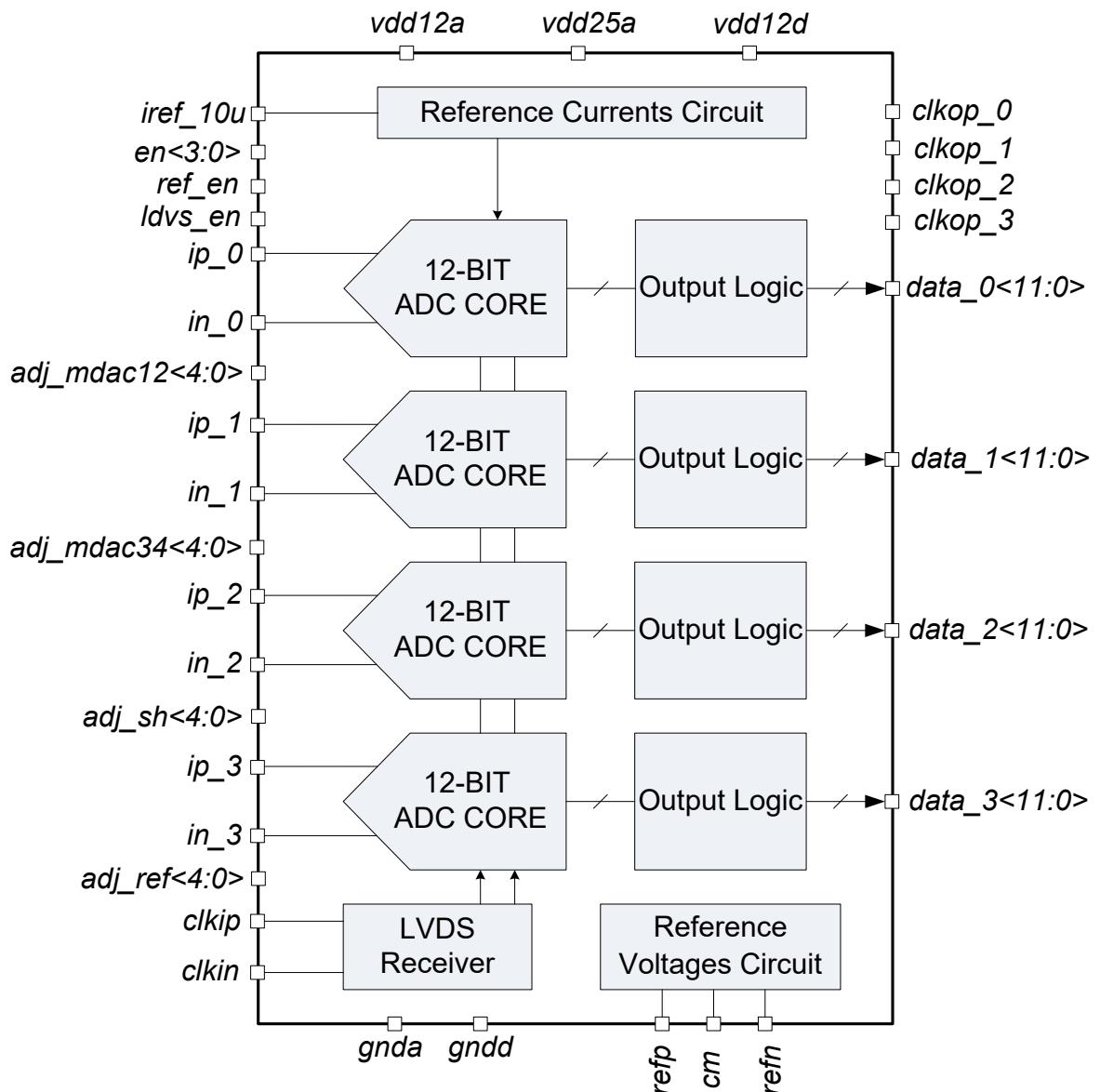


Figure 1: 12-bit 50/100/125 MSPS 4-channel ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
Analog Signals		
iref_10u	I	Reference current (10 uA)
ip_0	I	Differential analog inputs of channel 0
in_0	I	
ip_1	I	Differential analog inputs of channel 1
in_1	I	
ip_2	I	Differential analog inputs of channel 2
in_2	I	
ip_3	I	Differential analog inputs of channel 3
in_3	I	
refp	I/O	Differential reference voltages
refn	I/O	
cm	I/O	Common mode voltage
Digital inputs		
clkip	I	Differential clock input
clkin	I	
en<3:0>	I	Enables of ADCs
ref_en	I	Enable of reference voltages block
lvds_en	I	Enable of LVDS receiver
Digital outputs		
datap_0<11:0>	O	Output data of channel 0
datap_1<11:0>	O	Output data of channel 1
datap_2<11:0>	O	Output data of channel 2
datap_3<11:0>	O	Output data of channel 3
clkop_0	O	Output clock of channel 0
clkop_1	O	Output clock of channel 1
clkop_2	O	Output clock of channel 2
clkop_3	O	Output clock of channel 3
Test inputs		
adj_mdac12<4:0>	I	Bias control registers of MDACs
adj_mdac34<4:0>	I	
adj_sh<4:0>	I	Bias control registers of sample-and-hold circuit
adj_ref<4:0>	I	Reference voltages range control register
Supply Voltages		
vdd12a	I/O	Analog blocks supply voltage 1.2 V
vdd25a	I/O	Analog blocks supply voltage 2.5 V
vdd12d	I/O	Digital blocks supply voltage 1.2 V
gnda	I/O	Digital blocks ground
gnnd	I/O	Analog blocks ground

6 FUNCTIONAL DESCRIPTION

The analog input voltage is sampled t_{d1} time after the positive edge of the conversion clock. Digital output data is latched after the pipeline conversion latency of 4 clock cycles.

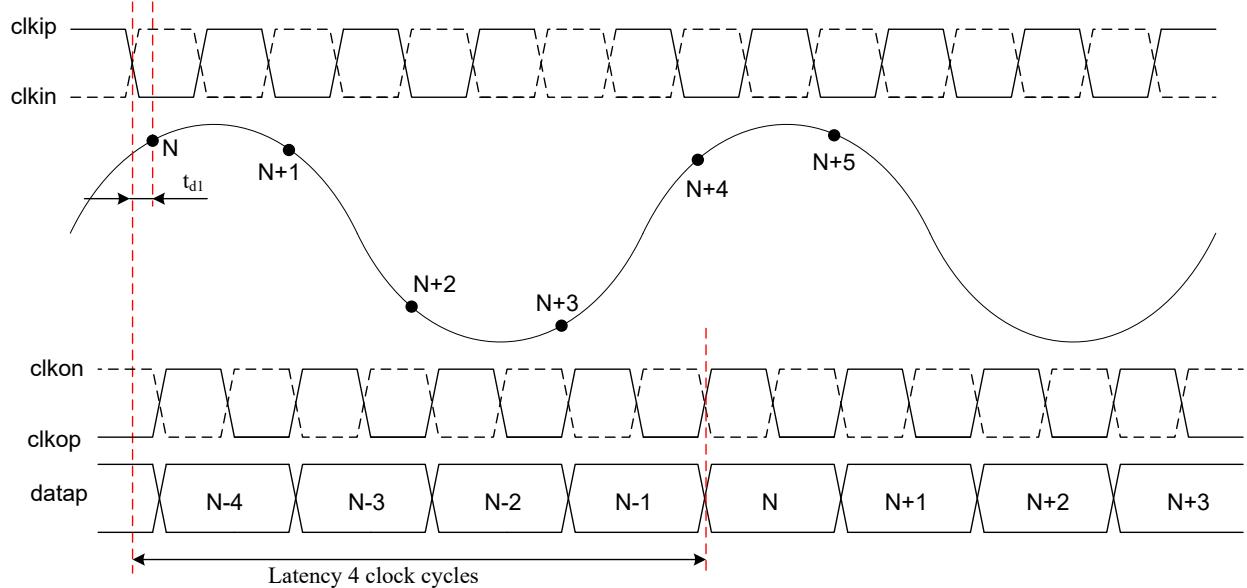


Figure 2: Timing diagram for normal operation

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

ADC is designed under TSMC 65 nm LP CMOS technology process with following options:

- 4x1z1u metal option
- 1.2 V standard V_t MOS
- 1.2 V low V_t MOS
- 2.0 fF/ μm^2 MIM capacitor
- P+ polysilicon OP resistor

7.2 PHYSICAL DIMENTIONS

ADC layout dimensions are given in the table 1.

Table 1: ADC dimensions.

Dimension	Value	Unit
Height	2398	um
Width	1910	um

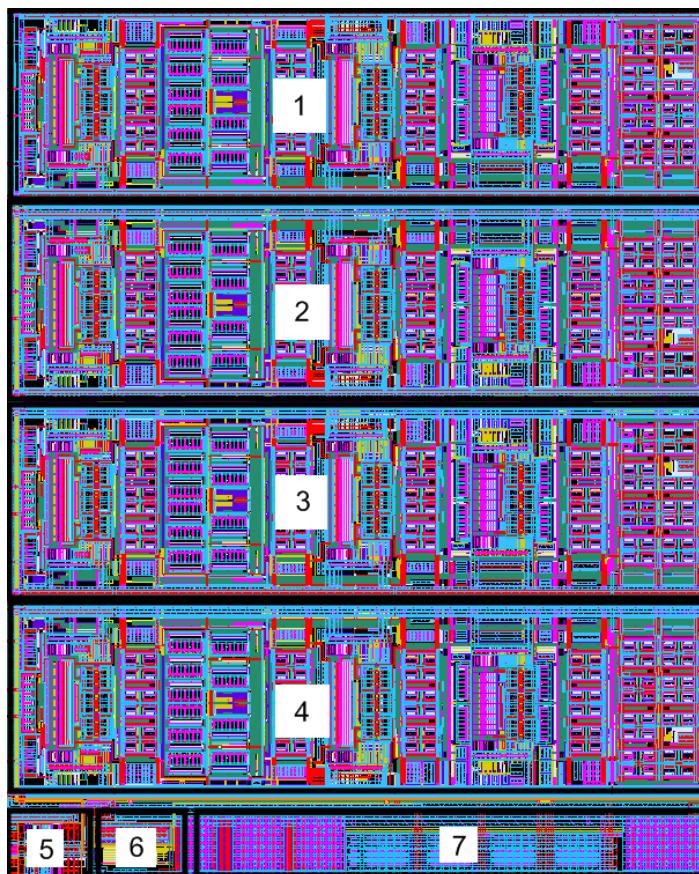


Figure 3: ADC layout view

1. ADC channel 0
2. ADC channel 1
3. ADC channel 2
4. ADC channel 3
5. LVDS receiver
6. Reference voltages block and reference current block
7. Capacitors on pins refp, cm and refn

8 INTEGRATION GUIDELINES

8.1 PLACE AND ROUTE GUIDELINES

- 1) ADC analog inputs ip and in signals should be connected to analog IO PADs or an internal analog circuits (intermediate frequency amplifier, filter). IO PADs should not have an internal resistor to increase bandwidth.
- 2) Wiring of analog inputs should be symmetrical and as short as possible.
- 3) Noisy, power and high-frequency circuits should not place near ADC.
- 4) Minimum space 40 um between ADC and other circuits should be kept.
- 5) Minimum ultra thick metal wiring width is 40 um for vdd12a and gnda. Multiple layers of metal can be used to reduce layout space.
- 6) Minimum ultra thick metal wiring width is 40 um for vdd12d and gndd. Multiple layers of metal can be used to reduce layout space.
- 7) Allowable total resistance of vdd12a and gnda are 0.1 Ohm. Blocking capacitors should be added and placed as close as possible.
- 8) Allowable total resistance of vdd12d and gndd are 0.2 Ohm. Blocking capacitors should be added and placed as close as possible.
- 9) The ADC requires off-chip capacitors on pins refp, cm and refn. The refp, cm and refn pins should be bypassed as shown in figure 4. The 100 nF capacitors between refp and refn should be as close to pins as possible.

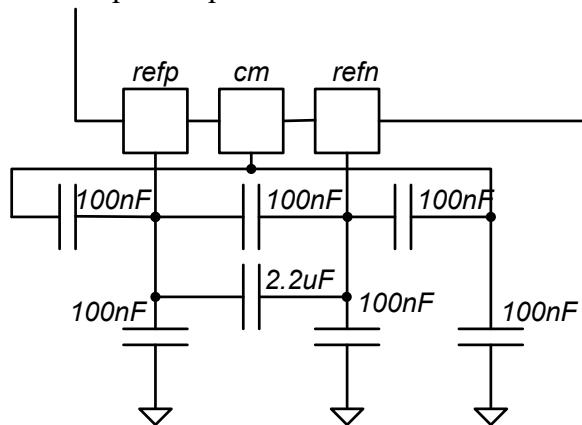


Figure 4: Capacitors on pins refp, cm and refn

9 OPERATING CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65 nm
 Status _____ silicon proven
 Area _____ 4.58 mm²

9.2 ELECTRICAL CHARACTERISTICS

The values of dynamic characteristics are specified for $V_{DDA} = V_{DDD} = 1.08 \div 1.32$ V, $V_{DDD25} = 2.25 \div 2.75$ V, $T_j = -40 \div 85^\circ\text{C}$, $A_{IN} = -1$ dBFS. Typical values are at $V_{DDA} = V_{DDD} = 1.2$ V, $V_{DDD25} = 2.5$ V, $T_j = +27^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Conditions	Value			Unit	
			min	typ.	max		
Junction temperature	T_j	-	-40	27	+85	°C	
Analog blocks supply voltage	V_{DDA}	-	1.08	1.2	1.32	V	
Digital blocks supply voltage	V_{DDD}	-	1.08	1.2	1.32	V	
Digital blocks supply voltage	V_{DDD25}	-	2.25	2.5	2.75	V	
Reference current	I_{REF}	-	9.9	10	10.1	uA	
Resolution	N	-	-	12	-	bit	
Sample rate	F_s	-	50	100	125	MHz	
Standby current	I_{ST}	-	-	40	-	uA	
Full power bandwidth	F_B	$F_s=50$ MHz or $F_s=100$ MHz	-	510	-	MHz	
Current consumption	I_{CN}	For four channels	$V_{DDA} + V_{DDD}$, $F_s = 50$ MHz	-	145	-	mA
			$V_{DDA} + V_{DDD}$, $F_s = 100$ MHz	-	210	-	mA
			$V_{DDA} + V_{DDD}$, $F_s = 125$ MHz	-	245	-	mA
	I_{CN25}	V_{DDD25}	-	1.6	-	mA	
Total power consumption	P_{TOTAL}	For four channels	$V_{DDA} + V_{DDD} + V_{DDD25}$, $F_s = 50$ MHz	-	178	-	mW
			$V_{DDA} + V_{DDD} + V_{DDD25}$, $F_s = 100$ MHz	-	256	-	mW
			$V_{DDA} + V_{DDD} + V_{DDD25}$, $F_s = 125$ MHz	-	298	-	mW
Differential input voltage range	A_{IN} p-p	-	-	1	-	V p-p	
Input common mode voltage	V_{CM}	-	-	0.6	-	V	
Differential reference voltages	V_{REFP}	-	-	0.85	-	V	
	V_{REFN}	-	-	0.35	-	V	

Table “Electrical characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Clock input duty cycle	S	-	45	50	55	%
Latency	T _{LAT}	-	-	4	-	clock cycles
Input logic high level	V _{IH}	For digital inputs	0.7 V _{DDD}	-	-	V
Input logic low level	V _{IL}		-	-	0.3 V _{DDD}	V

9.3 DYNAMIC CHARACTERISTICS

The values of dynamic characteristics are specified for $V_{DDA} = V_{DDD} = 1.08 \div 1.32$ V, $V_{DDD25} = 2.25 \div 2.75$ V, $T_j = -40 \div 85^\circ\text{C}$, $A_{IN} = -1$ dBFS. Typical values are at $V_{DDA} = V_{DDD} = 1.2$ V, $V_{DDD25} = 2.5$ V, $T_j = +27^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
$F_s = 50$ MHz						
Spurious free dynamic range	SFDR	$F_{IN} = 10.7$ MHz	65	73.7	75.5	dB
		$F_{IN} = 21.4$ MHz	65	73.7	75	
		$F_{IN} = 30.9$ MHz	67	73	74	
		$F_{IN} = 60.7$ MHz	65	66.5	69	
		$F_{IN} = 70.6$ MHz	64.5	65	68	
Total harmonic distortion	THD	$F_{IN} = 10.7$ MHz	72	77.4	82.5	dB
		$F_{IN} = 21.4$ MHz	72	81	82.5	
		$F_{IN} = 30.9$ MHz	70	77.3	78	
		$F_{IN} = 60.7$ MHz	68	70.7	75.7	
		$F_{IN} = 70.6$ MHz	70	75	77	
Signal-to-noise ratio	SNR	$F_{IN} = 10.7$ MHz	59.5	59.3	61.1	dB
		$F_{IN} = 21.4$ MHz	59.5	58	60.7	
		$F_{IN} = 30.9$ MHz	58.2	56.8	60.1	
		$F_{IN} = 60.7$ MHz	57.7	57.7	60	
		$F_{IN} = 70.6$ MHz	56.7	57	57.7	
Signal-to-noise and distortion ratio	SINAD (SNDR)	$F_{IN} = 10.7$ MHz	58.6	59.5	60	dB
		$F_{IN} = 21.4$ MHz	58	58.5	59.7	
		$F_{IN} = 30$ MHz	58	58.4	59.1	
		$F_{IN} = 60$ MHz	57	57.6	59	
		$F_{IN} = 70$ MHz	56.6	57	57.7	
Effective number of bits	ENOB	$F_{IN} = 10.7$ MHz	9.44	9.59	9.67	bits
		$F_{IN} = 21.4$ MHz	9.34	9.43	9.62	
		$F_{IN} = 30$ MHz	9.34	9.41	9.52	
		$F_{IN} = 60$ MHz	9.18	9.28	9.51	
		$F_{IN} = 70$ MHz	9.11	9.18	9.26	
Full power bandwidth	F _B	-	-	510	-	MHz
Differential nonlinearity	DNL	$F_{IN} = 10.7$ MHz	-	1.23	-	LSB
Integral nonlinearity	INL	$F_{IN} = 10.7$ MHz	-	2.74	-	LSB

Table “Dynamic characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
F_s = 100 MHz						
Spurious free dynamic range	SFDR	F _{IN} = 10.7 MHz	65	73.4	74.4	dB
		F _{IN} = 21.4 MHz	64	74.3	73	
		F _{IN} = 30.9 MHz	66	69.4	71.9	
		F _{IN} = 60.7 MHz	-	68	-	
		F _{IN} = 70.6 MHz	64	65.4	69	
Total harmonic distortion	THD	F _{IN} = 10.7 MHz	69	74.7	78.4	dB
		F _{IN} = 21.4 MHz	68	73.7	74	
		F _{IN} = 30.9 MHz	68	65.7	76	
		F _{IN} = 60.7 MHz	-	68	-	
		F _{IN} = 70.6 MHz	62	63	65	
Signal-to-noise ratio	SNR	F _{IN} = 10.7 MHz	60	59.3	61.8	dB
		F _{IN} = 21.4 MHz	59	59.7	60.9	
		F _{IN} = 30.9 MHz	59	60	61	
		F _{IN} = 60.7 MHz	-	58.8	-	
		F _{IN} = 70.6 MHz	57.5	59	60.2	
Signal-to-noise and distortion ratio	SINAD (SNDR)	F _{IN} = 10.7 MHz	58.5	59	60.2	dB
		F _{IN} = 21.4 MHz	57	58.5	59	
		F _{IN} = 30 MHz	57	57.8	58.7	
		F _{IN} = 60 MHz	-	58	-	
		F _{IN} = 70 MHz	57	57.6	58.5	
Effective number of bits	ENOB	F _{IN} = 10.7 MHz	9.43	9.51	9.71	bits
		F _{IN} = 21.4 MHz	9.18	9.43	9.51	
		F _{IN} = 30 MHz	9.18	9.31	9.46	
		F _{IN} = 60 MHz	-	9.34	-	
		F _{IN} = 70 MHz	9.18	9.28	9.43	
Full power bandwidth	F _B	-	-	510	-	MHz
Differential nonlinearity	DNL	F _{IN} = 10.7 MHz	-	1.1	-	LSB
Integral nonlinearity	INL	F _{IN} = 10.7 MHz	-	3.34	-	LSB

Table “Dynamic characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
F_s = 125 MHz						
Spurious free dynamic range	SFDR	F _{IN} = 10.7 MHz	-	70.5	-	dB
		F _{IN} = 21.4 MHz	-	70.8	-	
		F _{IN} = 60 MHz	-	67.6	-	
Total harmonic distortion	THD	F _{IN} = 10.7 MHz	-	67.2	-	dB
		F _{IN} = 21.4 MHz	-	68.5	-	
		F _{IN} = 60 MHz	-	72.2	-	
Signal-to-noise ratio	SNR	F _{IN} = 10.7 MHz	-	58	-	dB
		F _{IN} = 21.4 MHz	-	58.1	-	
		F _{IN} = 60 MHz	-	58.9	-	
Signal-to-noise and distortion ratio	SINAD (SNDR)	F _{IN} = 10.7 MHz	-	58	-	dB
		F _{IN} = 21.4 MHz	-	58.4	-	
		F _{IN} = 60 MHz	-	58.3	-	
Effective number of bits	ENOB	F _{IN} = 10.7 MHz	-	9.34	-	bits
		F _{IN} = 21.4 MHz	-	9.4	-	
		F _{IN} = 60 MHz	-	9.4	-	

10 TYPICAL CHARACTERISTICS

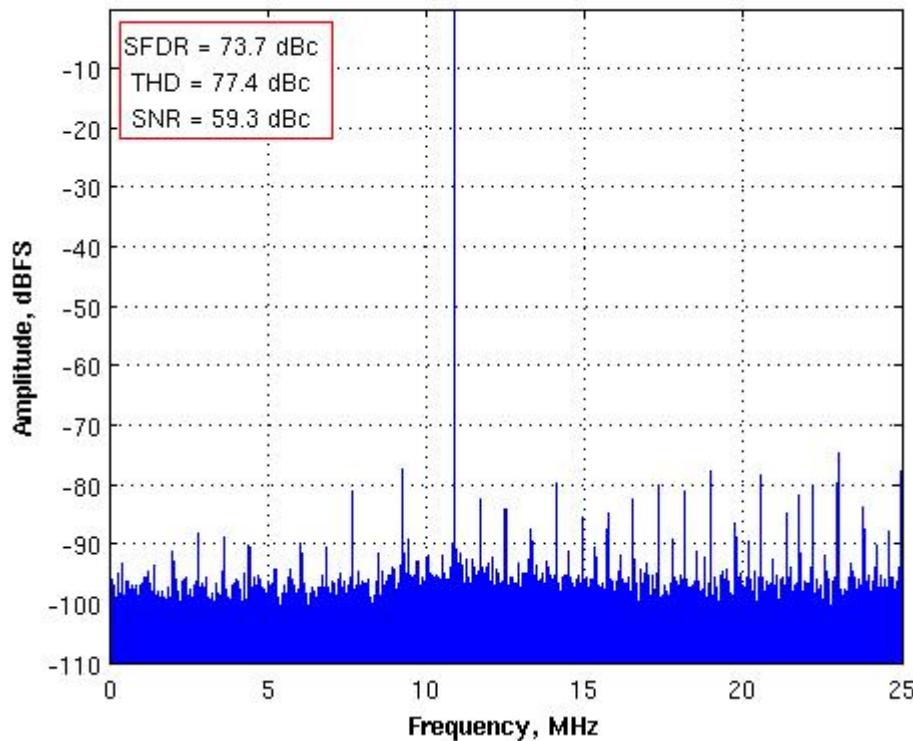


Figure 5: Single-tone FFT with $F_{IN} = 10.7$ MHz, $F_s = 50$ MHz,
 $A_{IN} = -1$ dBFS

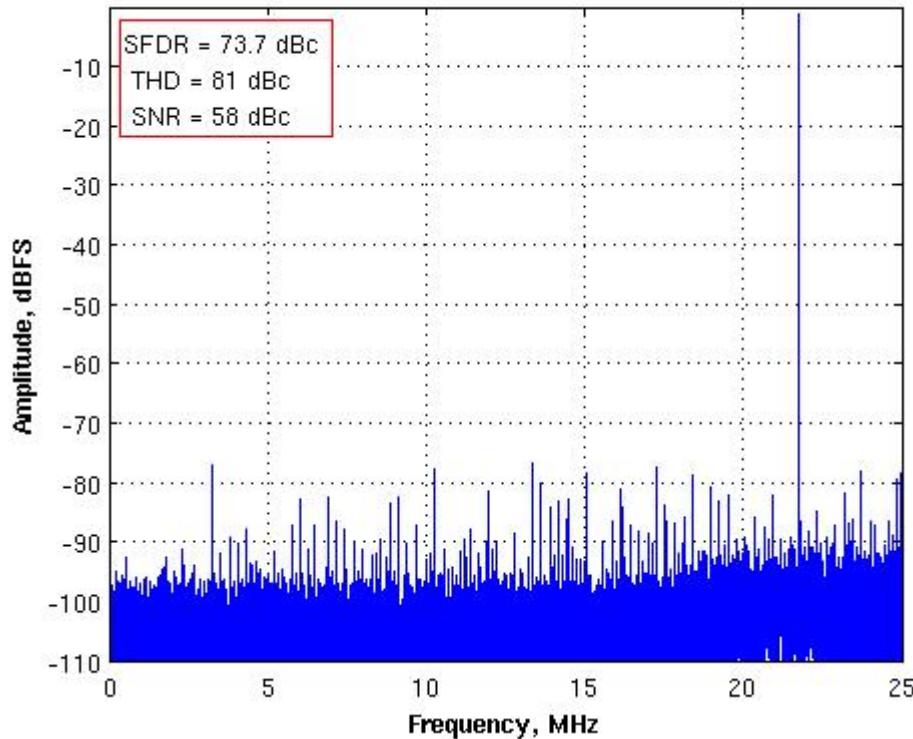


Figure 6: Single-tone FFT with $F_{IN} = 21.4$ MHz, $F_s = 50$ MHz,
 $A_{IN} = -1$ dBFS

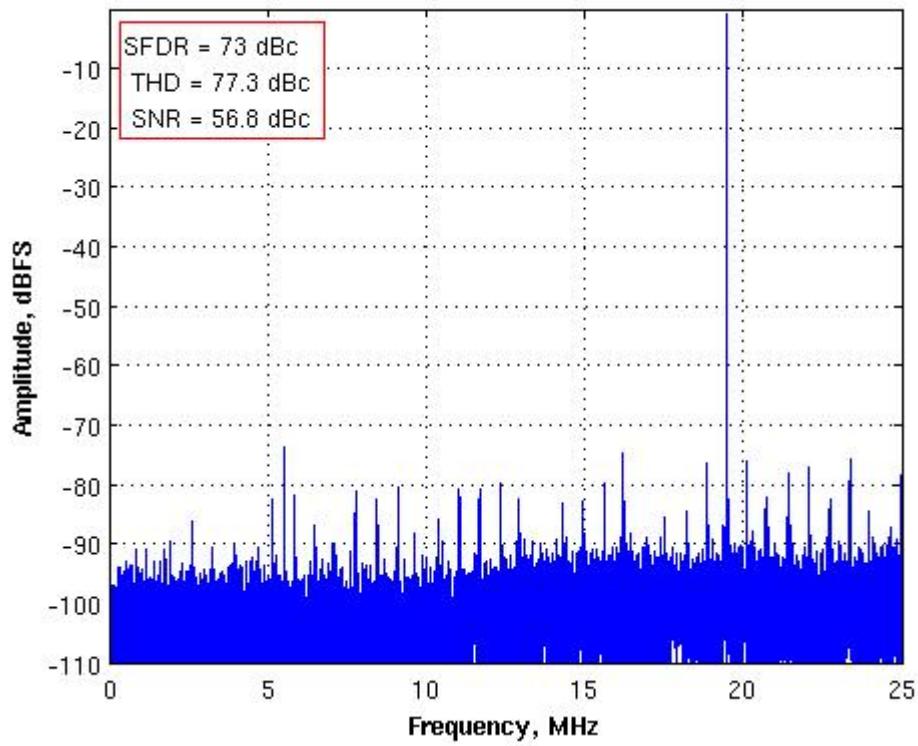


Figure 7: Single-tone FFT with $F_{IN} = 30.9$ MHz, $F_s = 50$ MHz,
 $A_{IN} = -1$ dBFS

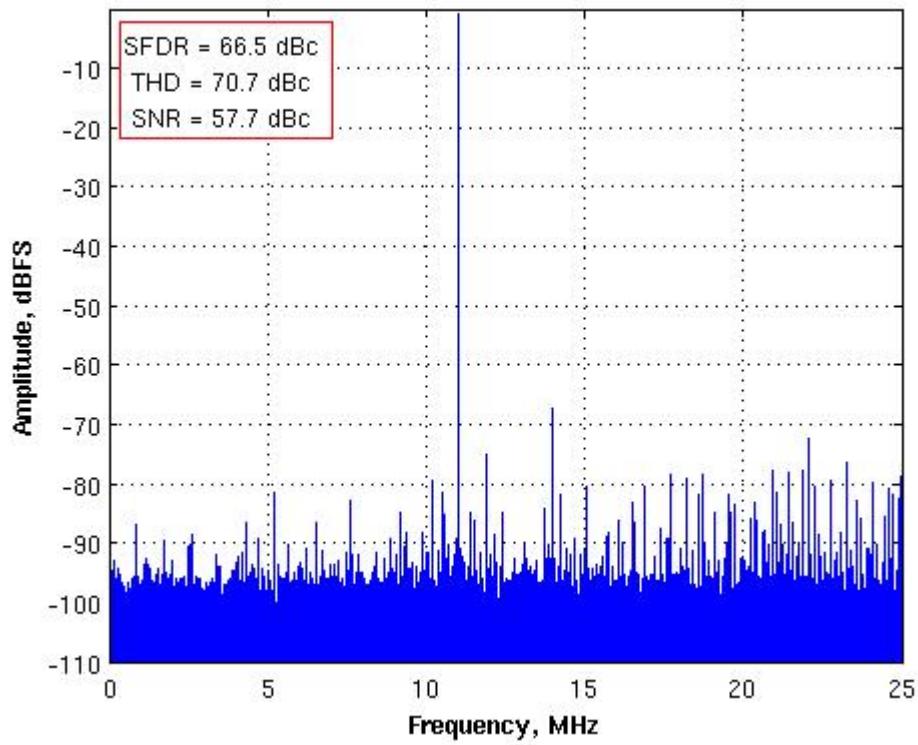


Figure 8: Single-tone FFT with $F_{IN} = 60.7$ MHz, $F_s = 50$ MHz,
 $A_{IN} = -1$ dBFS

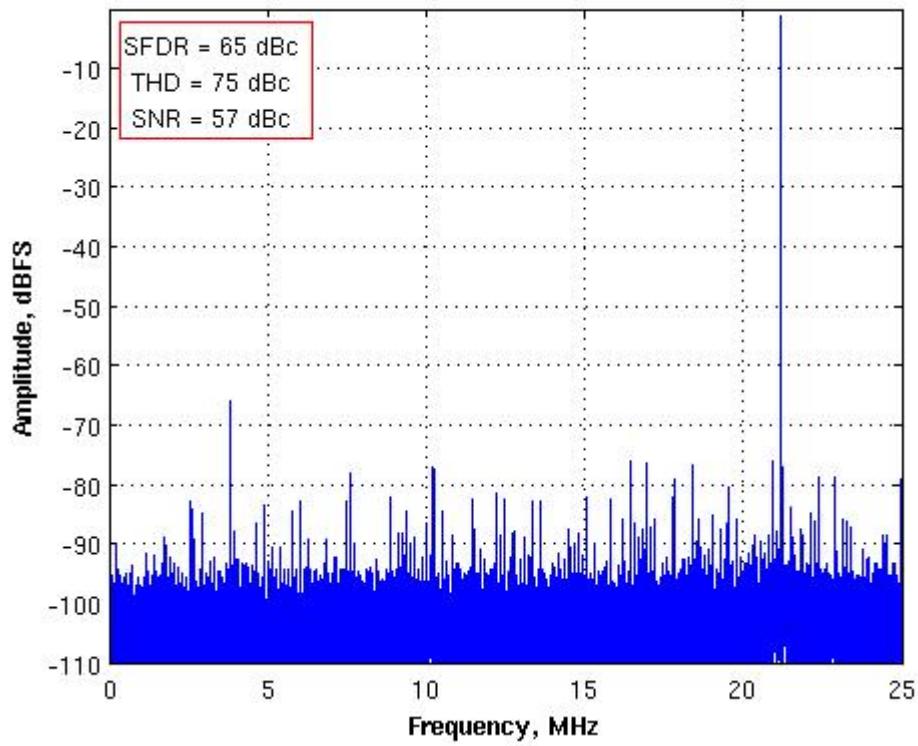


Figure 9: Single-tone FFT with $F_{IN} = 70.6$ MHz, $F_S = 50$ MHz,
 $A_{IN} = -1$ dBFS

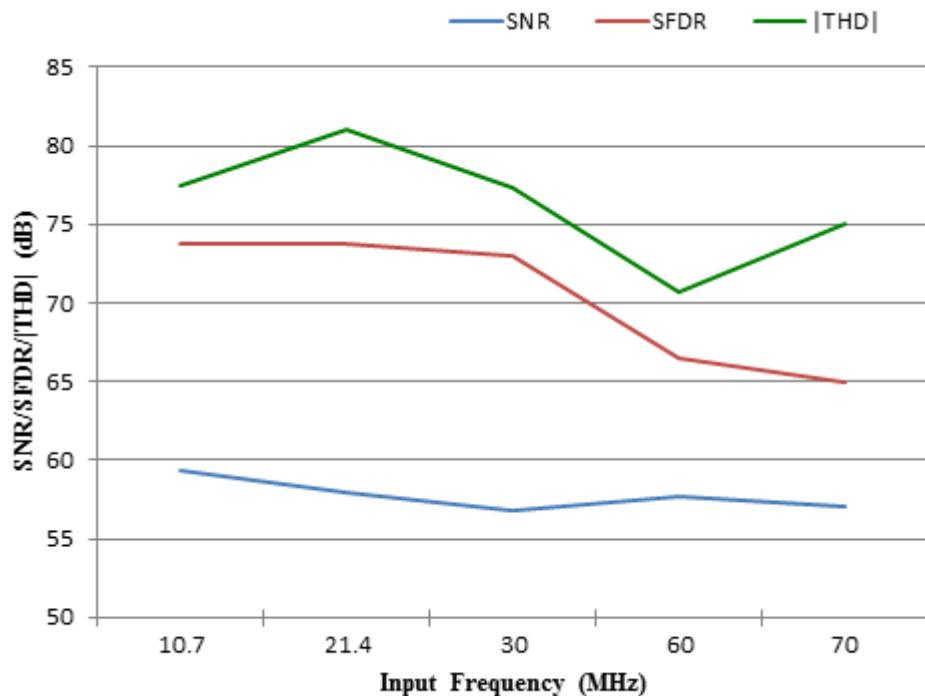


Figure 10: SNR/THD/SFDR vs. F_{IN} , $F_S = 50$ MHz,
 $A_{IN} = -1$ dBFS

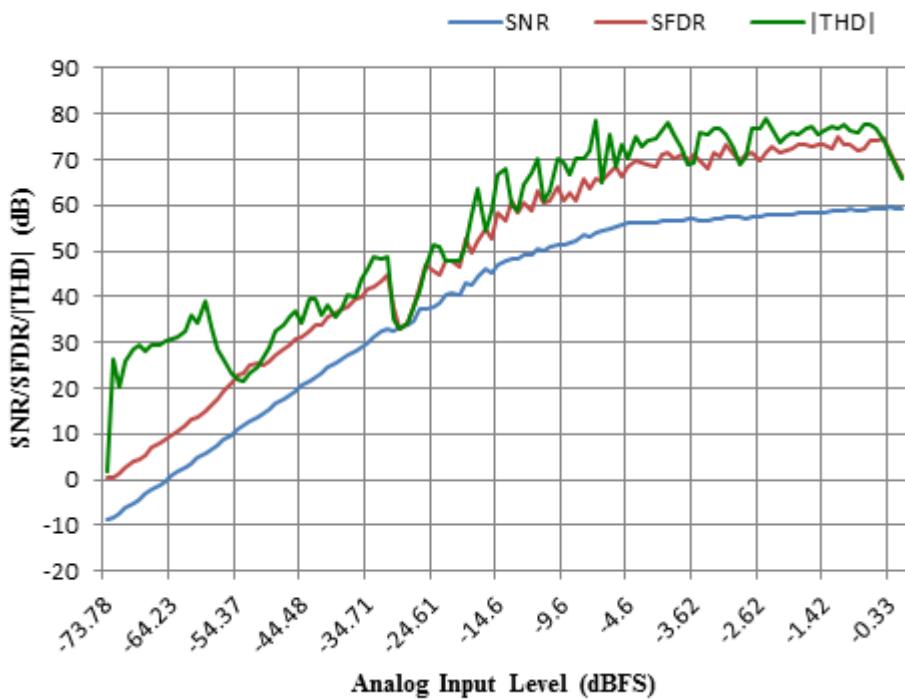


Figure 11: SNR/THD/SFDR vs. analog input level, $F_{IN} = 10.7$ MHz, $F_S = 50$ MHz

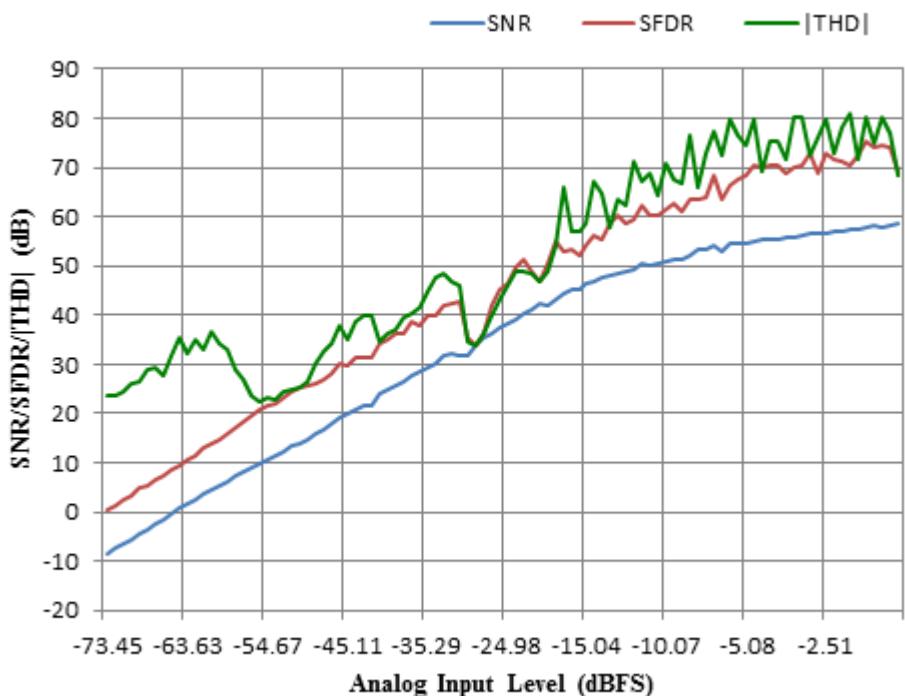


Figure 12: SNR/THD/SFDR vs. analog input level, $F_{IN} = 21.4$ MHz, $F_S = 50$ MHz

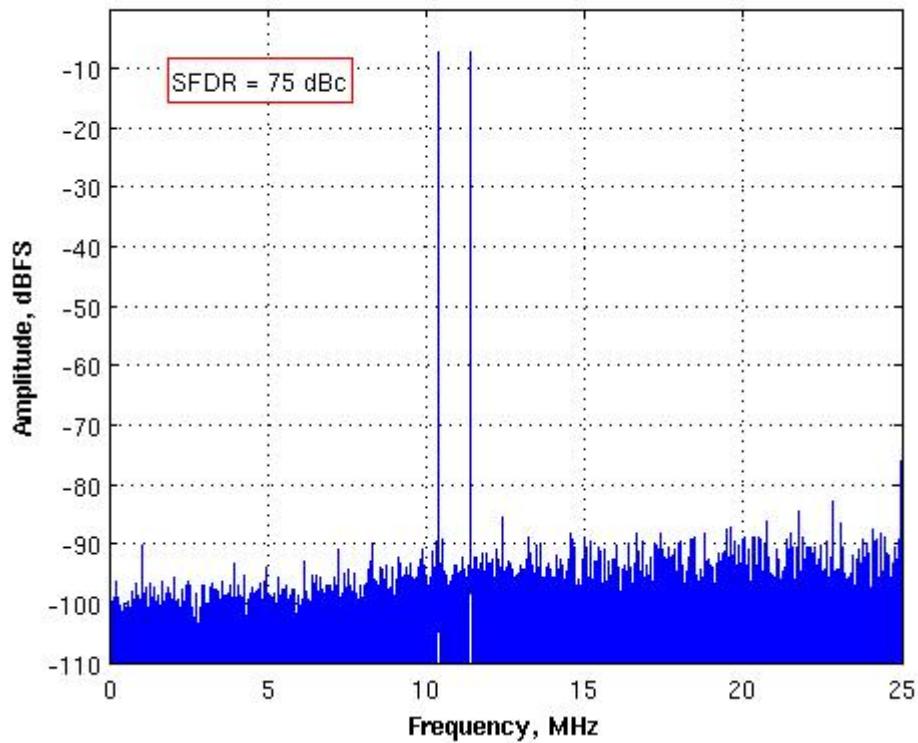


Figure 13: Two-tone FFT with $F_{IN1} = 10.2$ MHz, $F_{IN2} = 11.2$ MHz, $F_S = 50$ MHz,
 $A_{IN} = -7$ dBFS

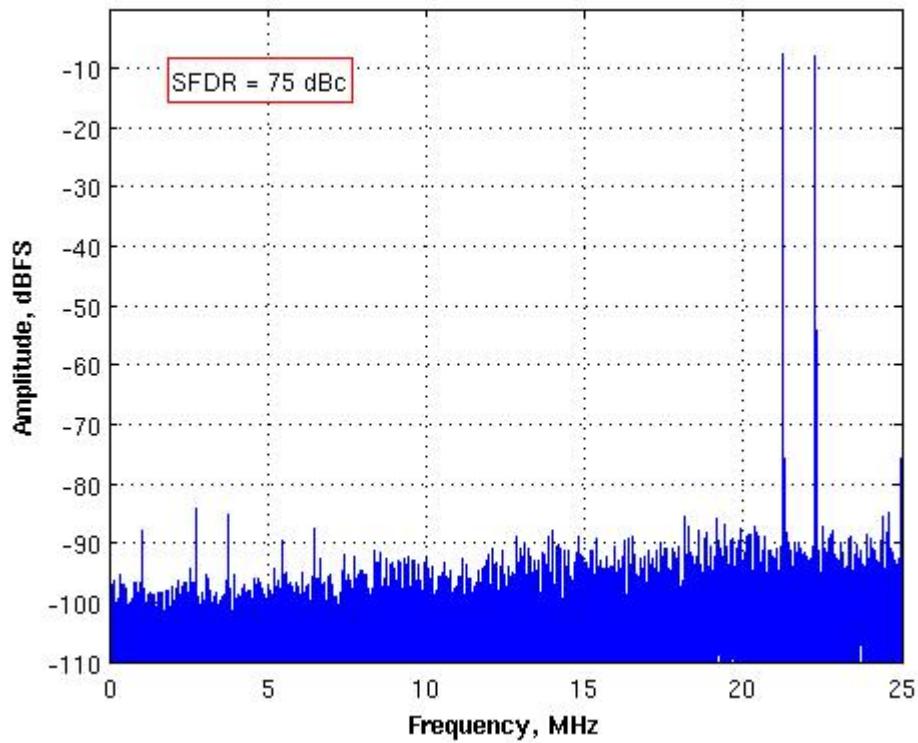


Figure 14: Two-tone FFT with $F_{IN1} = 20.9$ MHz, $F_{IN2} = 21.9$ MHz, $F_S = 50$ MHz,
 $A_{IN} = -7$ dBFS

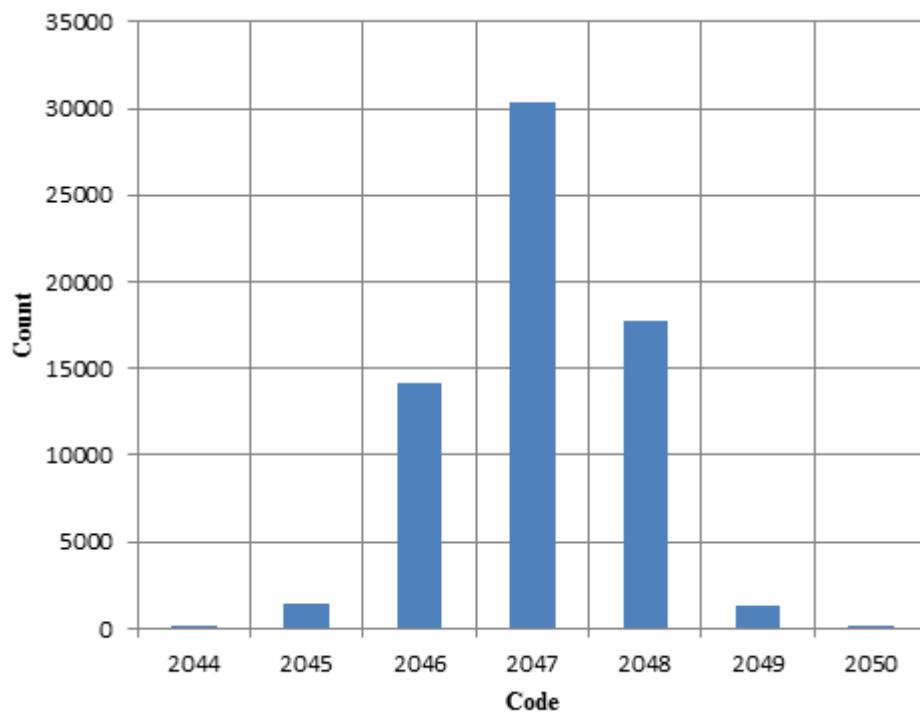


Figure 15: Grounded input histogram, $F_s = 50$ MHz

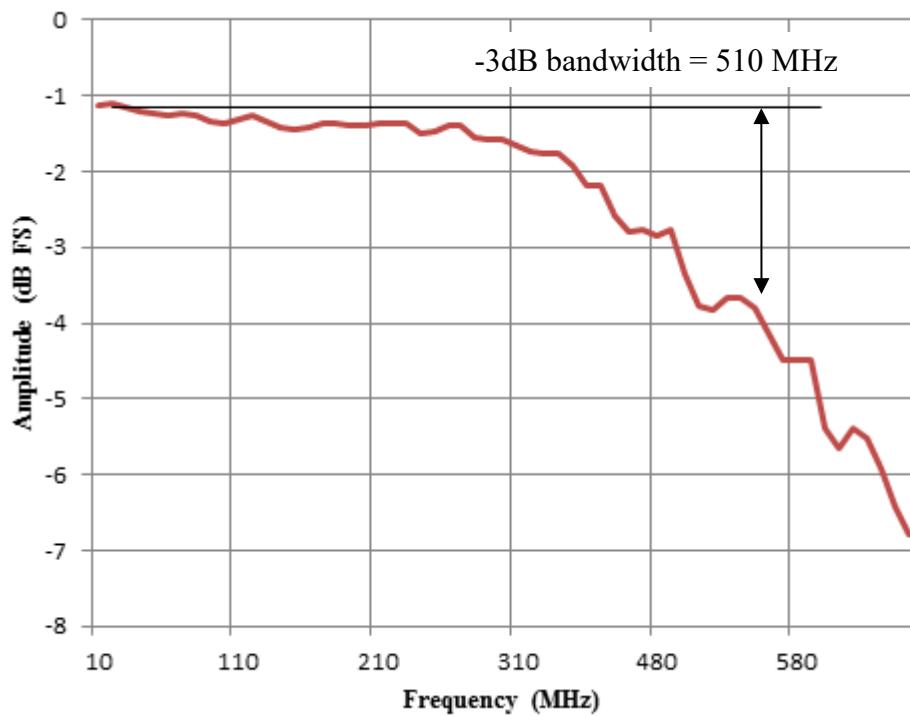


Figure 16: Full-power bandwidth vs. frequency, $F_s = 50$ MHz

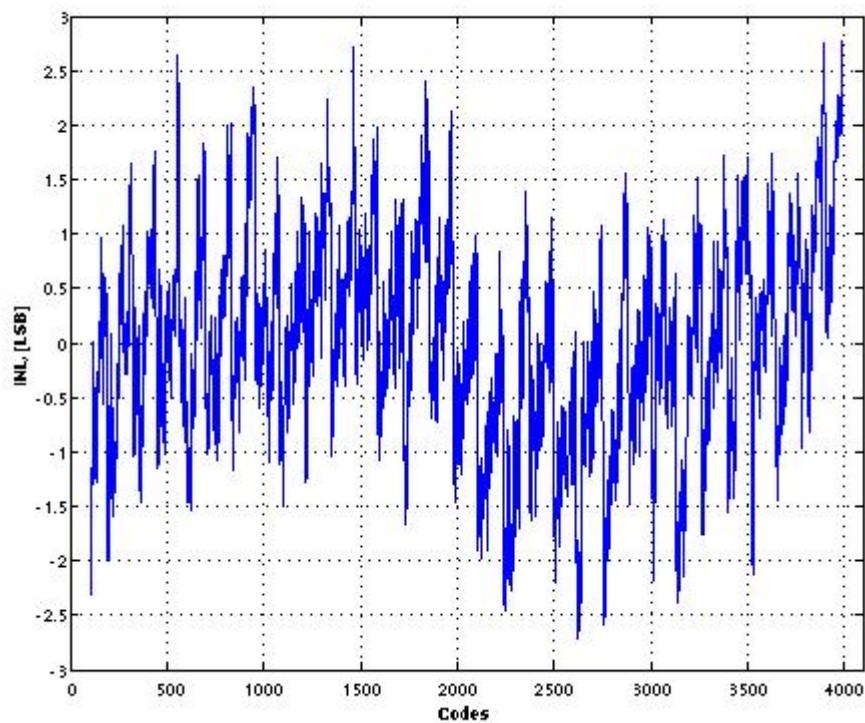


Figure 17: Integral nonlinearity (INL), $F_{IN} = 10.7$ MHz, $F_s = 50$ MHz

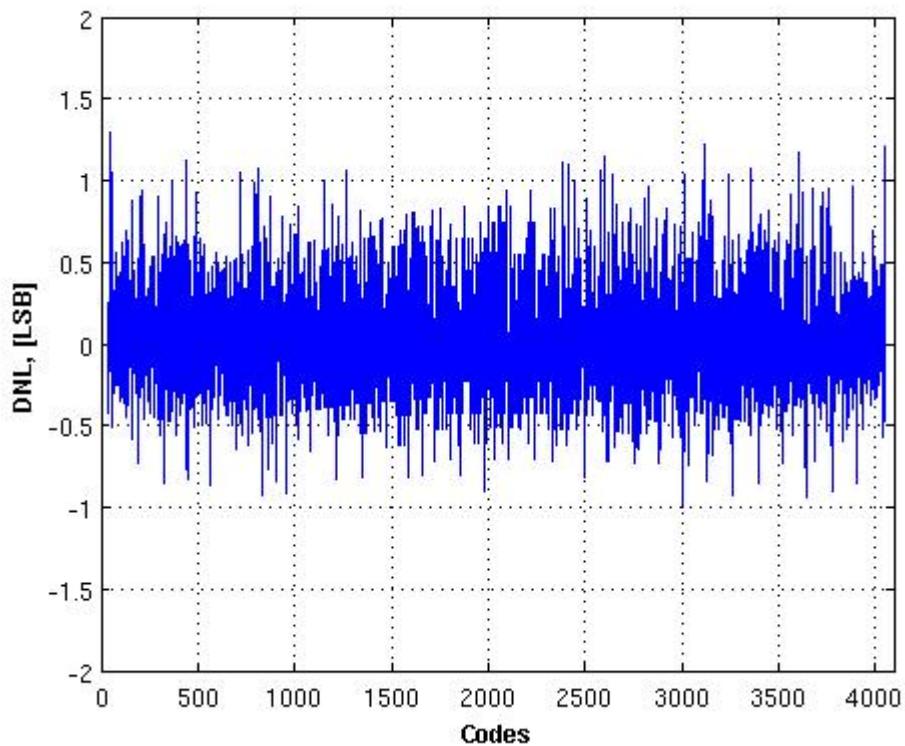


Figure 18: Differential nonlinearity (DNL), $F_{IN} = 10.7$ MHz, $F_s = 50$ MHz

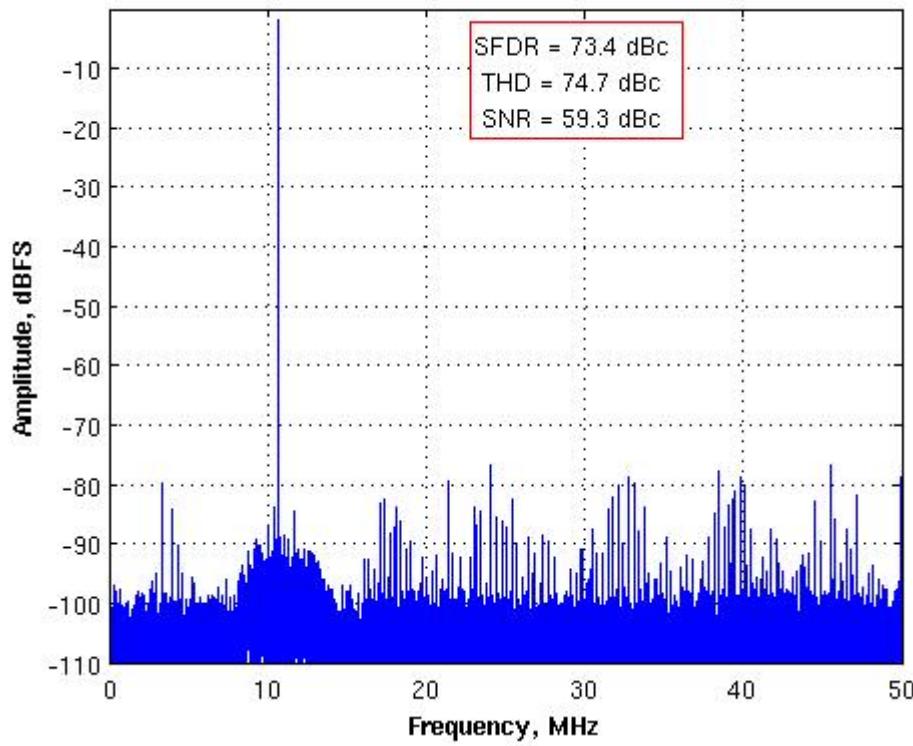


Figure 19: Single-tone FFT with $F_{IN} = 10.7$ MHz, $F_s = 100$ MHz,
 $A_{IN} = -1$ dBFS

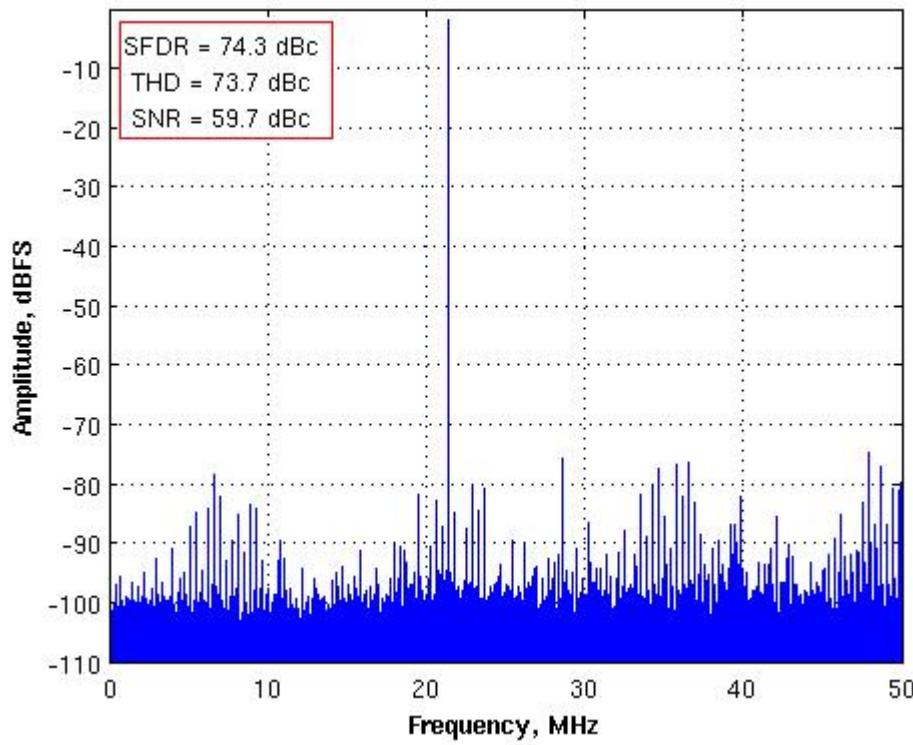


Figure 20: Single-tone FFT with $F_{IN} = 21.4$ MHz, $F_s = 100$ MHz,
 $A_{IN} = -1$ dBFS

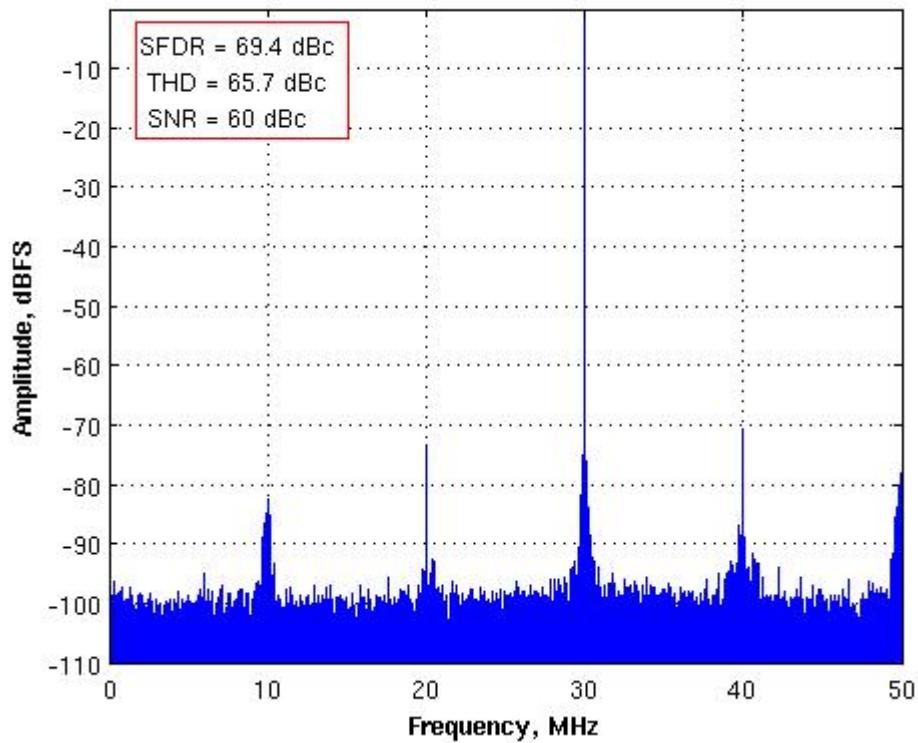


Figure 21: Single-tone FFT with $F_{IN} = 30$ MHz, $F_s = 100$ MHz,
 $A_{IN} = -1$ dBFS

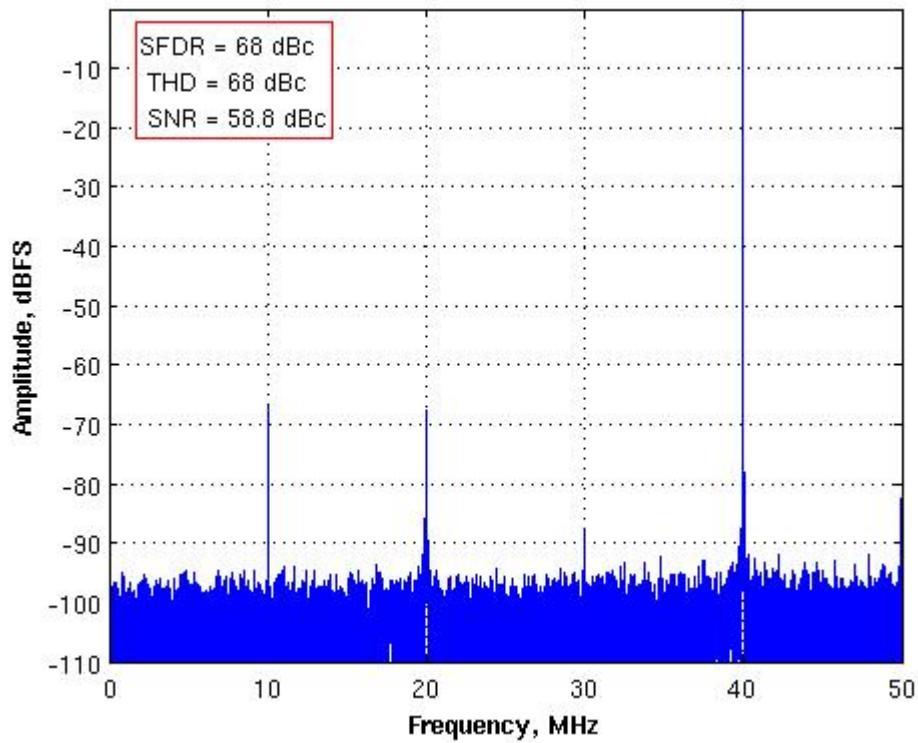


Figure 22: Single-tone FFT with $F_{IN} = 60$ MHz, $F_s = 100$ MHz,
 $A_{IN} = -1$ dBFS

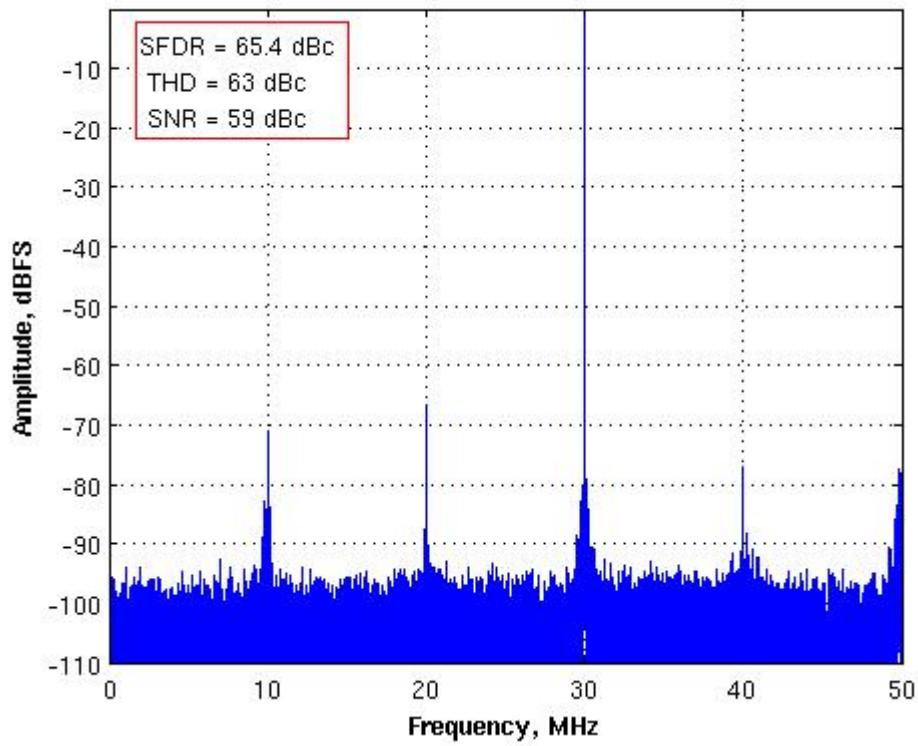


Figure 23: Single-tone FFT with $F_{IN} = 70$ MHz, $F_S = 100$ MHz,
 $A_{IN} = -1$ dBFS

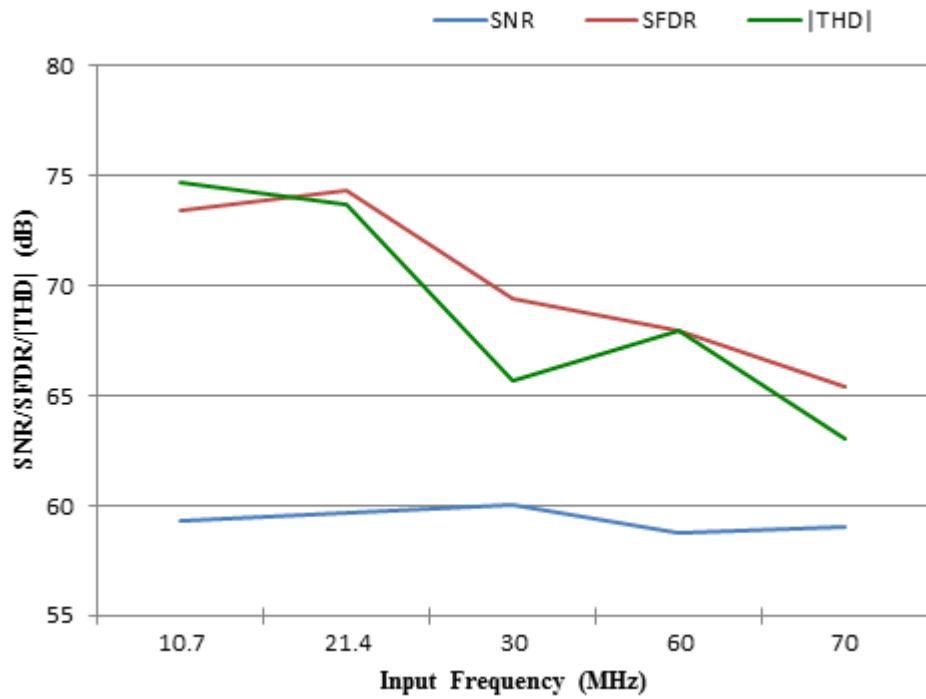


Figure 24: SNR/THD/SFDR vs. F_{IN} , $F_S = 100$ MHz

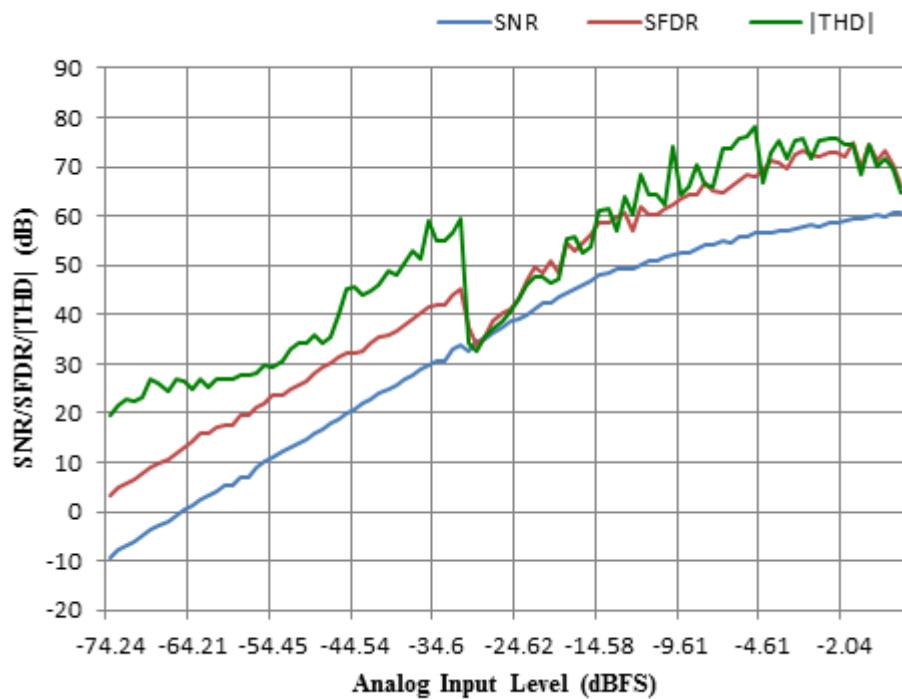


Figure 25: SNR/THD/SFDR vs. analog input level, $F_{IN} = 10.7$ MHz, $F_S = 100$ MHz

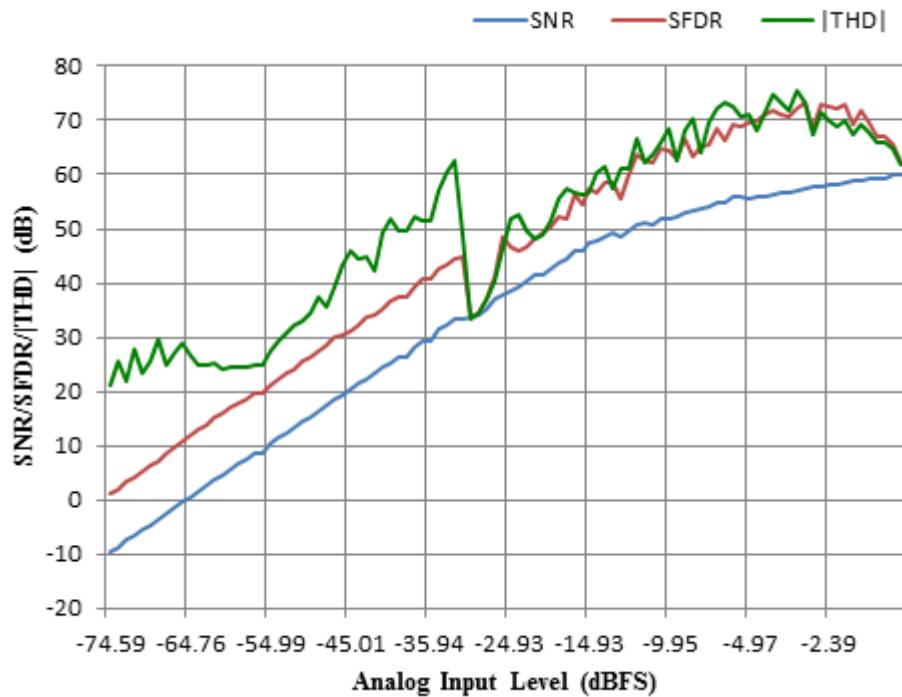


Figure 26: SNR/THD/SFDR vs. analog input level, $F_{IN} = 21.4$ MHz, $F_S = 100$ MHz

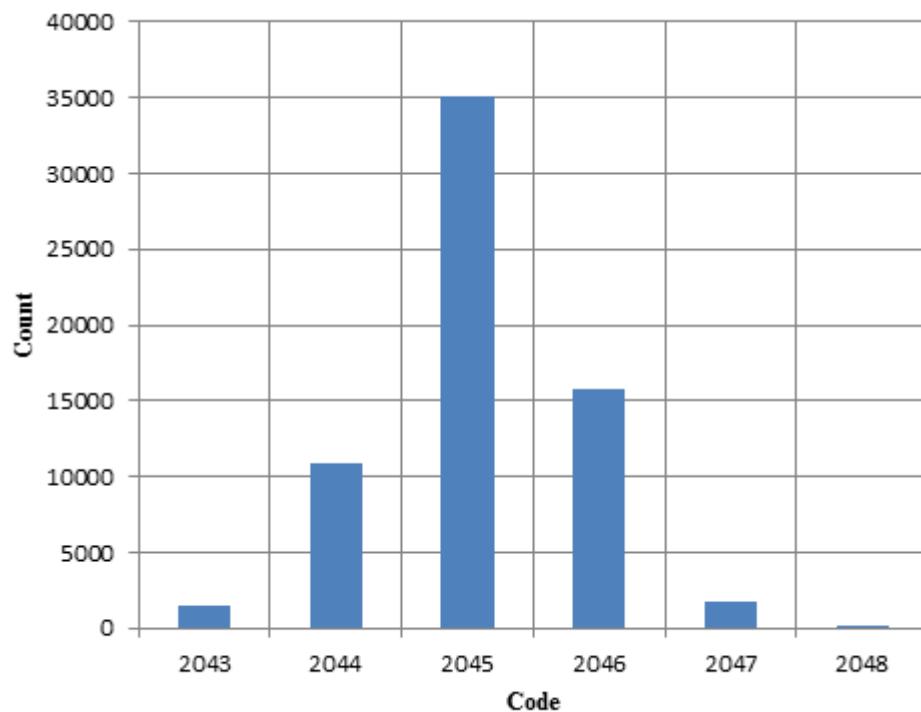


Figure 27: Grounded input histogram, $F_S = 100$ MHz

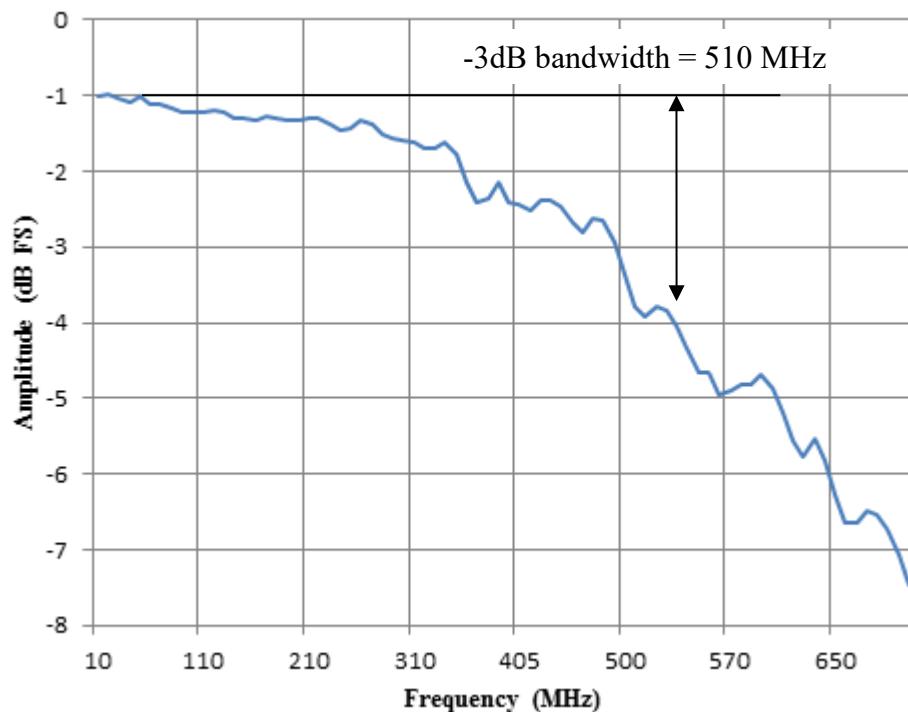


Figure 28: Full-power bandwidth vs. frequency, $F_S = 100$ MHz

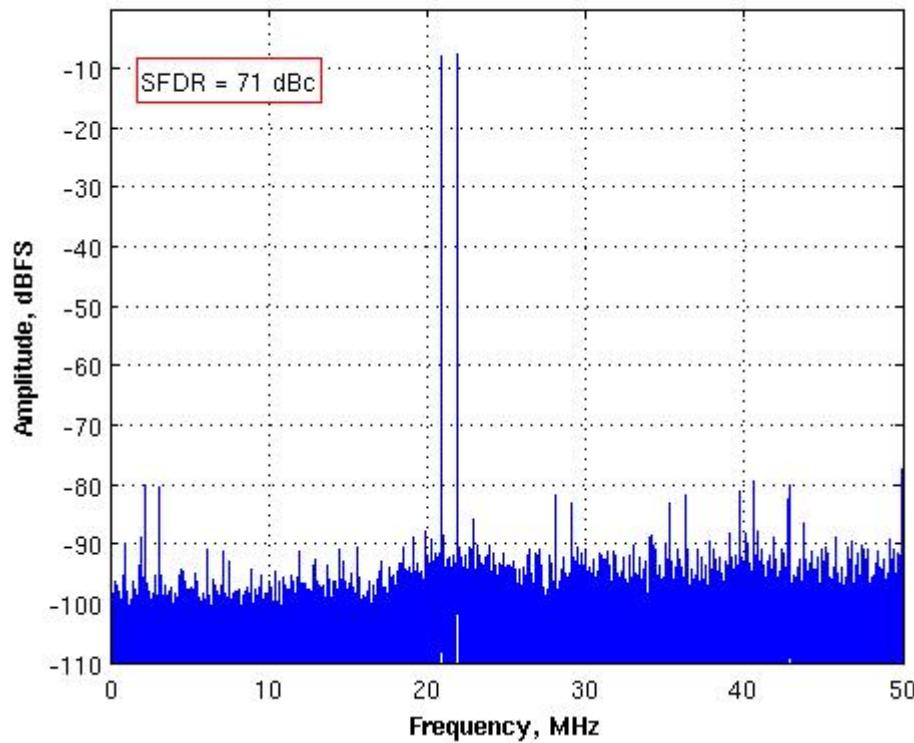


Figure 29: Two-tone FFT with $F_{IN1} = 20.9$ MHz, $F_{IN2} = 21.9$ MHz, $F_S = 100$ MHz,
 $A_{IN} = -7$ dBFS

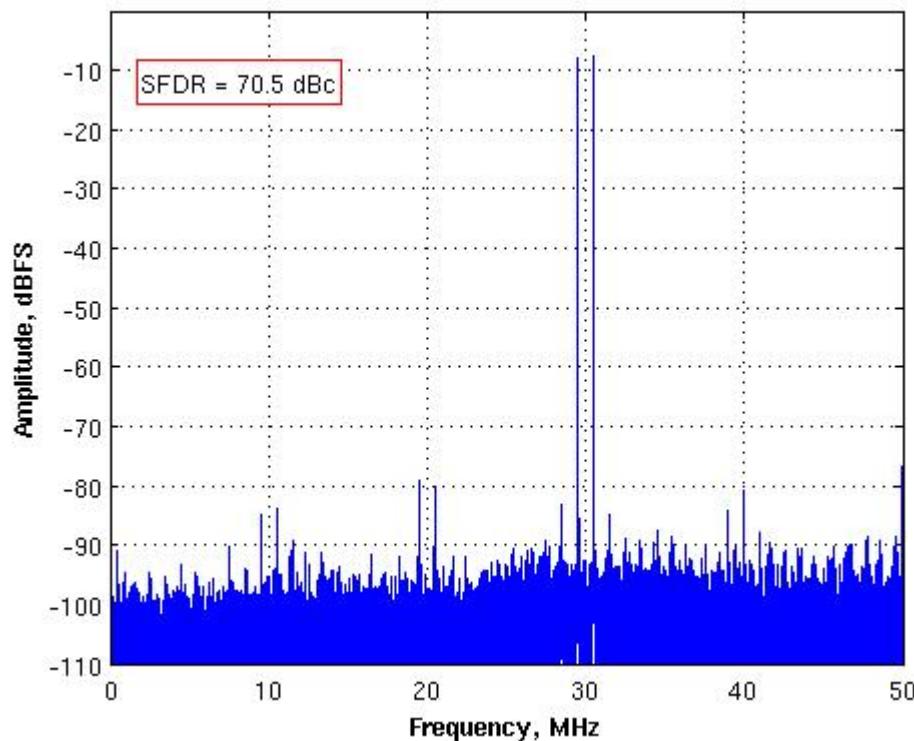


Figure 30: Two-tone FFT with $F_{IN1} = 29.5$ MHz, $F_{IN2} = 30.5$ MHz, $F_S = 100$ MHz,
 $A_{IN} = -7$ dBFS

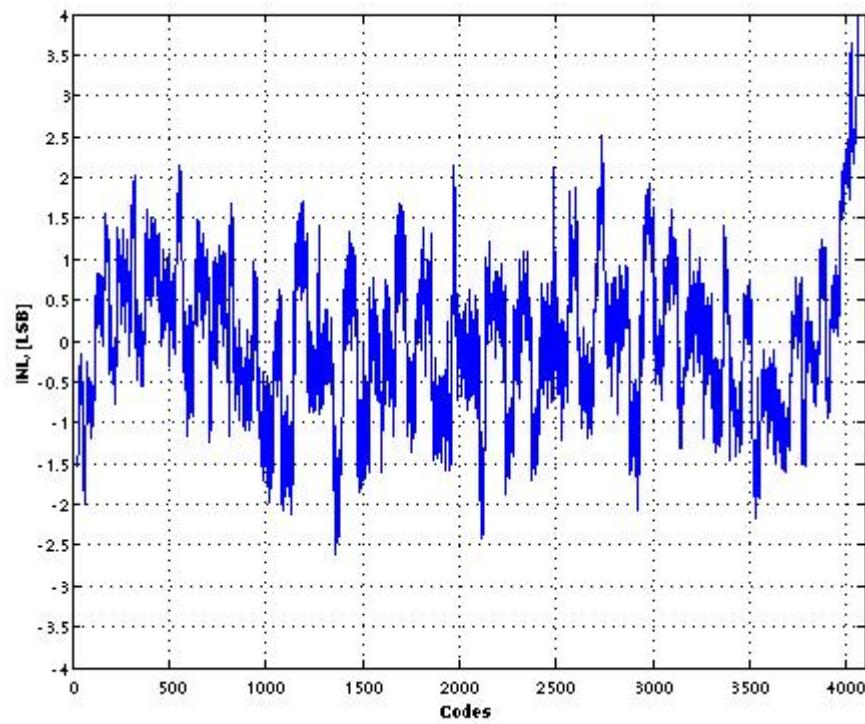


Figure 31: Integral nonlinearity (INL), $F_{IN} = 10.7$ MHz, $F_S = 100$ MHz

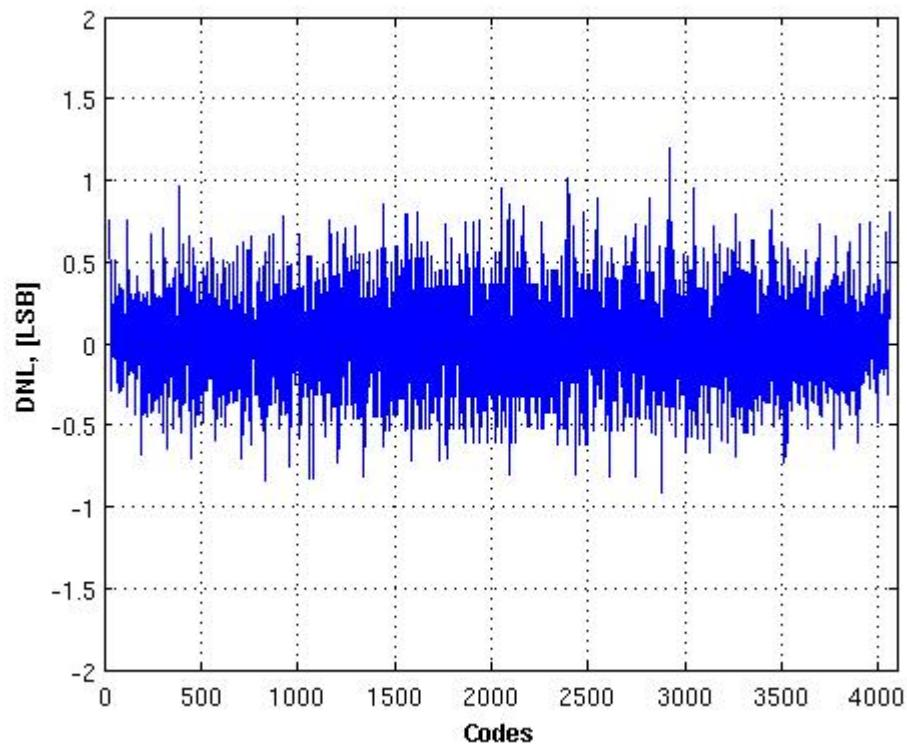


Figure 32: Differential nonlinearity (DNL), $F_{IN} = 10.7$ MHz, $F_S = 100$ MHz

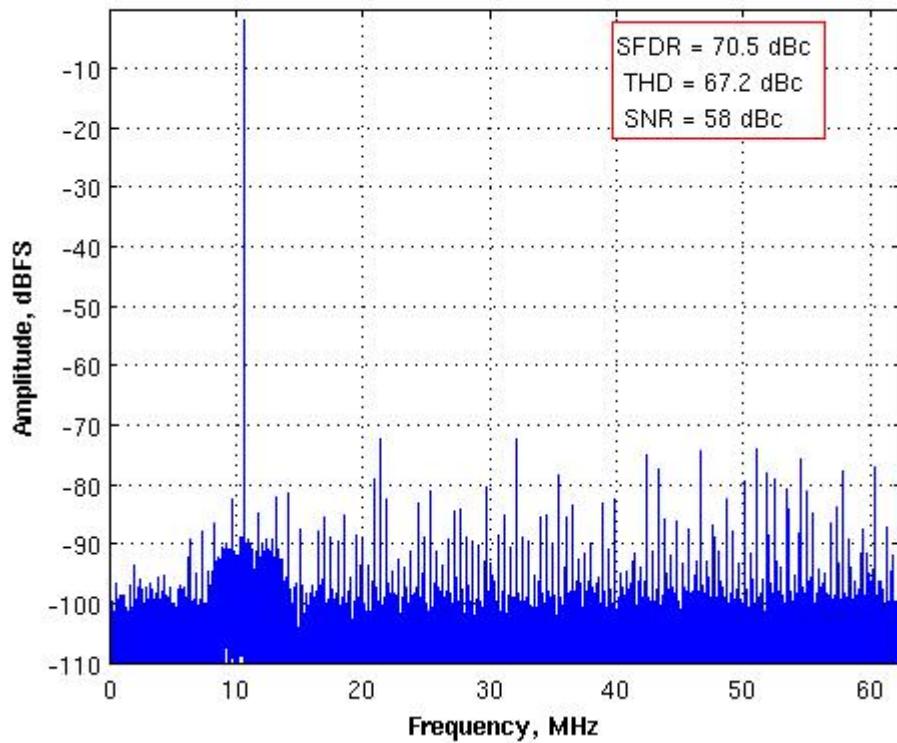


Figure 33: Single-tone FFT with $F_{IN} = 10.7$ MHz, $F_s = 125$ MHz,
 $A_{IN} = -1$ dBFS

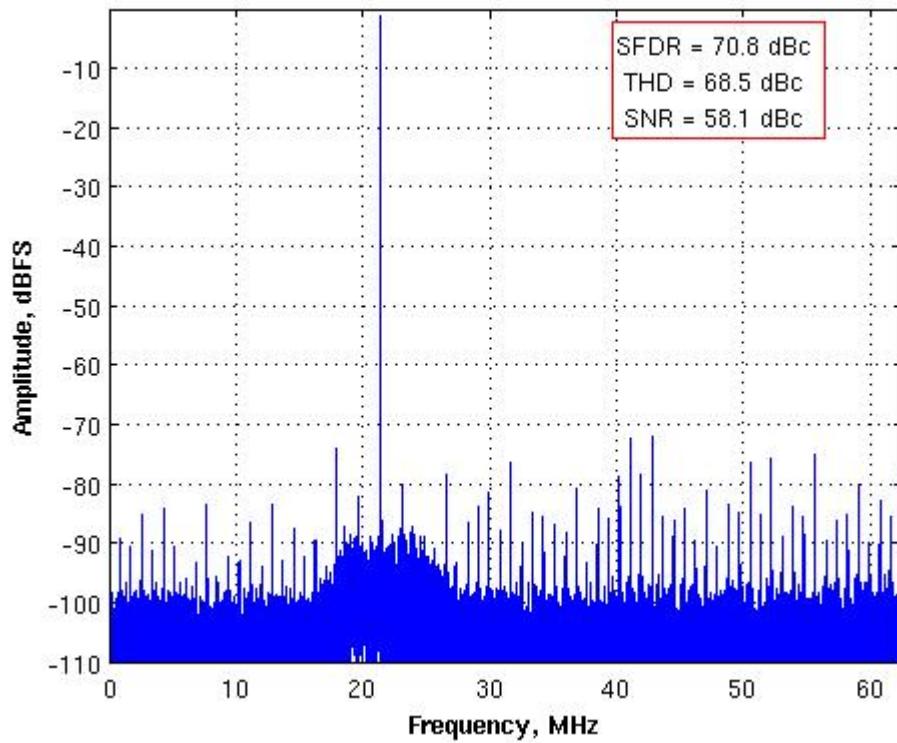


Figure 34: Single-tone FFT with $F_{IN} = 21.4$ MHz, $F_s = 125$ MHz,
 $A_{IN} = -1$ dBFS

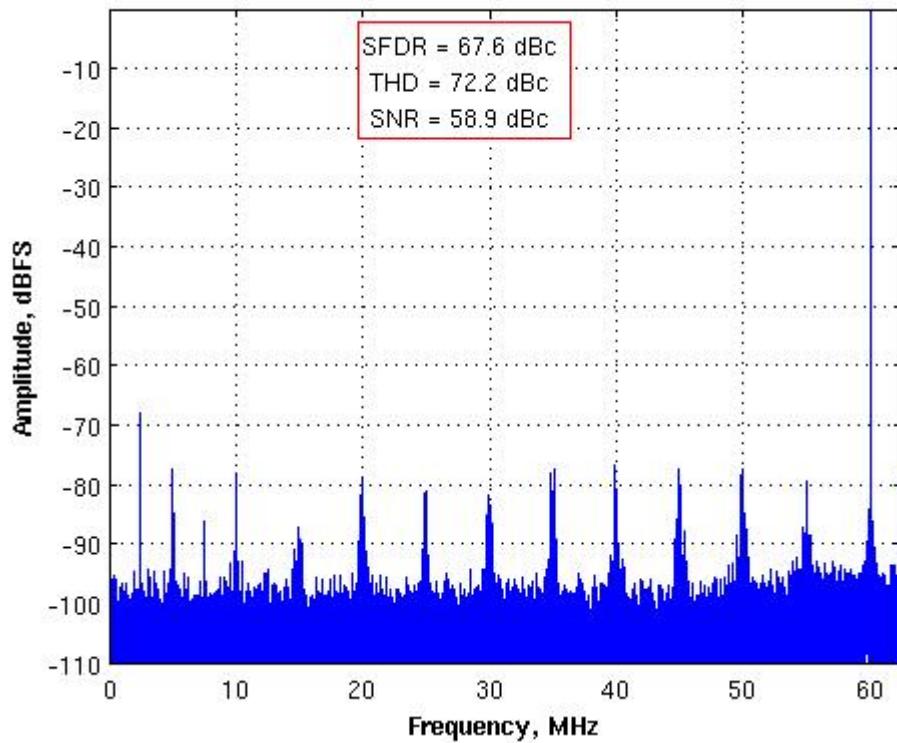


Figure 35: Single-tone FFT with $F_{IN} = 60$ MHz, $F_s = 125$ MHz,
 $A_{IN} = -1$ dBFS

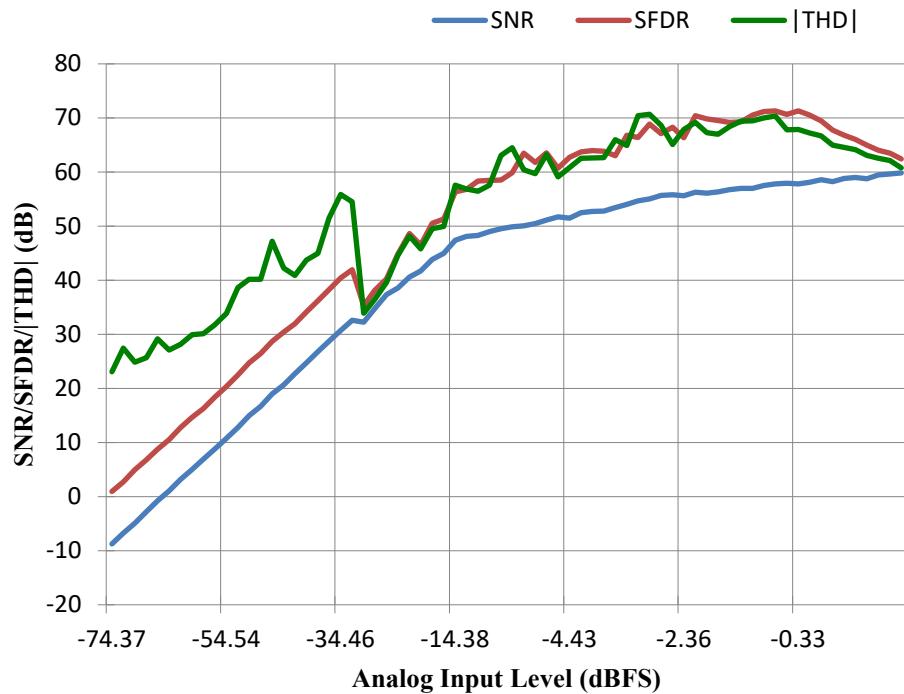


Figure 36: SNR/SFDR/|THD| vs. analog input level, $F_{IN} = 21.4$ MHz, $F_s = 125$ MHz

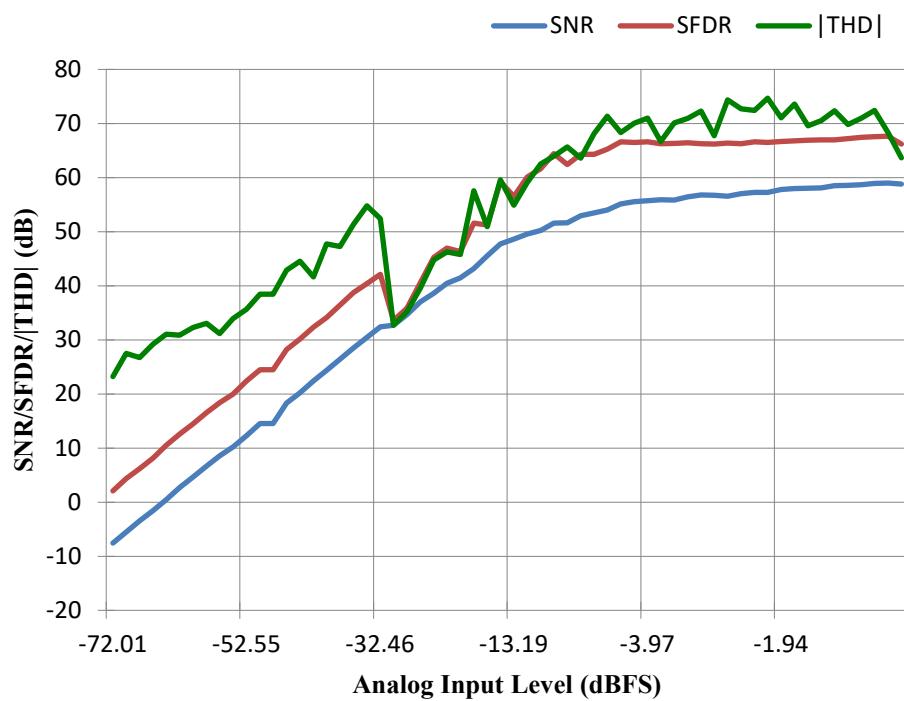


Figure 37: SNR/THD/SFDR vs. analog input level, $F_{IN} = 60$ MHz, $F_s = 125$ MHz

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.0:

- Section 1 changed
- Section 3 changed
- Subsection 7.2 changed
- Section 8 shifted to section 9
- Section 8 added
- Subsection 9.1 changed
- Subsection 9.2 changed
- Subsection 9.3 changed