12-bit 50/100/125 MSPS 4-channel pipeline ADC

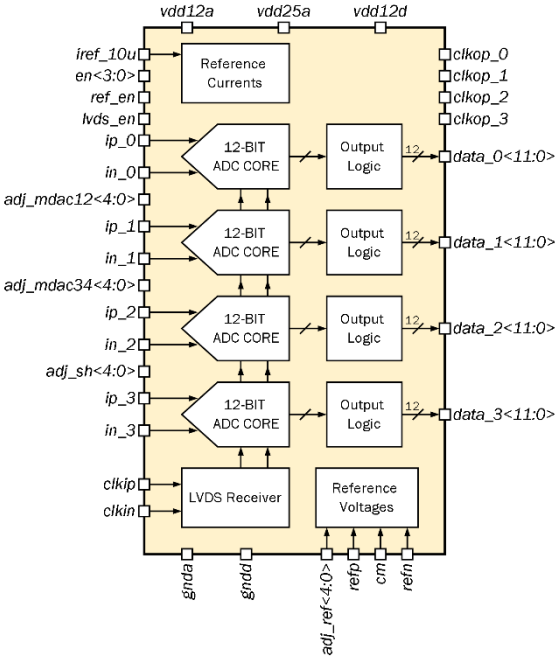
OVERVIEW

065TSMC_ADC_11 employs a high-performance differential pipeline architecture. The ADC consists of LVDS receiver, reference currents circuit, reference voltage circuit and 4 channels, which contain a core ADC and output logic. The ADC requires: 1.08 ÷ 1.32 V analog supply, 1.08 ÷ 1.32 V digital supply, reference current 9.9 ÷ 10.1 uA and differential input clock. The ADC supports standby mode which does possible state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.

IP technology: TSMC CMOS 65 nm.

IP status: silicon proven.

Area: 4.58mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog blocks supply voltage	V_{dd12a}	-		1.08	1.2	1.32	V
Digital blocks supply voltage	V_{dd12d}	-		1.08	1.2	1.32	V
	V_{dd25d}	-		2.25	2.5	2.75	V
Junction temperature	T_j	-		-40	+27	+85	°C
Resolution	N	-		-	12	-	bit
Sample rate	F_S	-		50	100	125	MSPS
Current consumption	I_{CC}	For four channels	V_{dd12a}+V_{dd12d}, F_S=50MSPS	-	145	-	mA
			V_{dd12a}+V_{dd12d}, F_S=100MSPS	-	210	-	mA
			V_{dd12a}+V_{dd12d}, F_S=125MSPS	-	245	-	mA
		@V_{dd25d}		-	1.6	-	mA
Differential input voltage range	$A_{IN\ p\text{-}p}$	-		-	1	-	Vp-p
Input common mode voltage	V_{CM}	-		-	0.6	-	V
Spurious free dynamic range	SFDR	F_S = 50MSPS	F_{IN} = 10.7MHz	65	73.7	75.5	dB
			F_{IN} = 21.4MHz				
		F_S = 100MSPS	F_{IN} = 10.7MHz	65	73.4	74.4	dB
			F_{IN} = 21.4MHz	64	74.3	73	
		F_S = 125MSPS	F_{IN} = 10.7MHz	-	70.8	-	dB
			F_{IN} = 21.4MHz	-		-	
Signal-to-noise ratio	SNR	F_S = 50MSPS	F_{IN} = 10.7MHz	59.5	59.3	61.1	dB
			F_{IN} = 21.4MHz				
		F_S = 100MSPS	F_{IN} = 10.7MHz	60	59.3	61.8	dB
			F_{IN} = 21.4MHz	59	59.7	60.9	
		F_S = 125MSPS	F_{IN} = 10.7MHz	-	58	-	dB
			F_{IN} = 21.4MHz	-	58.1	-	
Full power bandwidth	F_B	@50MSPS; @100MSPS		-	510	-	MHz
Differential nonlinearity	DNL	F_S = 50MSPS	F_{IN} = 10.7MHz	-	1.23	-	LSB
		F_S = 100MSPS		-	1.1	-	LSB
Integral nonlinearity	INL	F_S = 50MSPS	F_{IN} = 10.7MHz	-	2.74	-	LSB
		F_S = 100MSPS		-	3.34	-	LSB
Input logic high level	V_{IH}	For digital inputs		0.7 V_{dd12d}	-	V_{dd12d}	V
Input logic low level	V_{IL}			0	-	0.3 V_{dd12d}	V