12-bit 50/100/125 MSPS 1-channel pipeline ADC

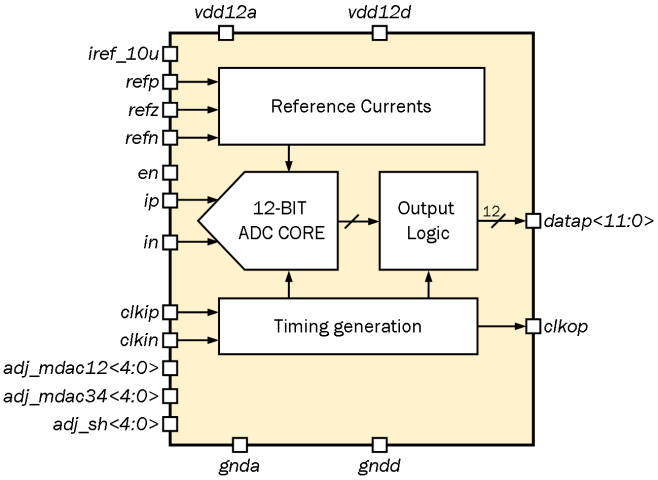
OVERVIEW

The low-power high-speed 12-bit ADC employs a high-performance differential pipeline architecture. The ADC consists of a core ADC, output logic, timing generation and reference currents circuits. The ADC requires: 1.08 ÷ 1.32 V analog supply, 1.08 ÷ 1.32 V digital supply, reference current 10 uA, differential reference voltages 0.85 V and 0.35 V, common mode voltage 0.6 V and differential input clock. The ADC supports standby mode which do possible state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.

IP technology: TSMC CMOS 65 nm.

IP status: silicon proven.

Area: 1.03mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog blocks supply voltage	V_{dd12a}	-		1.08	1.2	1.32	V
Digital blocks supply voltage	V_{dd12d}	-		1.08	1.2	1.32	V
Junction temperature	T_j	-		-40	+27	+85	°C
Reference current	I_{REF}	-		9.9	10	10.1	uA
Resolution	N	-		-	12	-	bit
Sample rate	F_S	-		50	100	125	MHz
Standby current	I_{ST}	-		-	9.5	-	uA
Current consumption	I_{CC}	V_{dd12a}+V_{dd12d}, F_S = 50 MHz		33	34	35.5	mA
		V_{dd12a}+V_{dd12d}, F_S = 100 MHz		47.6	50.2	52.3	mA
		V_{dd12a}+V_{dd12d}, F_S = 125 MHz		-	59	-	mA
Differential input voltage range	$A_{IN\ p\text{-}p}$	-		-	1	-	V p-p
Input common mode voltage	V_{CM}	-		-	0.6	-	V
Differential reference voltages	V_{REFP}	-		-	0.85	-	V
	V_{REFN}	-		-	0.35	-	V
Clock input duty cycle	S	-		45	50	55	%
Spurious free dynamic range	SFDR	F_S = 50 MHz	F_{IN} = 10.7 MHz	65	73.7	75.5	dB
			F_{IN} = 21.4 MHz	65	73.7	75	
		F_S = 100 MHz	F_{IN} = 10.7 MHz	65	73.4	74.4	dB
			F_{IN} = 21.4 MHz	64	74.3	73	
		F_S = 125 MHz	F_{IN} = 10.7 MHz	-	70.5	-	dB
			F_{IN} = 21.4 MHz	-	70.8	-	
Signal-to-noise ratio	SNR	F_S = 50 MHz	F_{IN} = 10.7 MHz	59.5	59.3	61.1	dB
			F_{IN} = 21.4 MHz	59.5	58	60.7	
		F_S = 100 MHz	F_{IN} = 10.7 MHz	60	59.3	61.8	dB
			F_{IN} = 21.4 MHz	59	59.7	60.9	
		F_S = 125 MHz	F_{IN} = 10.7 MHz	-	58	-	dB
			F_{IN} = 21.4 MHz	-	58.1	-	
Full power bandwidth	F_B	@50/100 MSPS		-	510	-	MHz
Differential nonlinearity	DNL	F_S = 50 MHz	F_{IN} = 10.7 MHz	-	±1.17	-	LSB
		F_S = 100 MHz		-	±1.18	-	LSB
Integral nonlinearity	INL	F_S = 50 MHz	F_{IN} = 10.7 MHz	-	±2.74	-	LSB
		F_S = 100 MHz		-	±3.9	-	LSB
Input logic high level	V_{IH}	For digital inputs		0.7 V_{dd12d}	-	V_{dd12d}	V
Input logic low level	V_{IL}			0	-	0.3 V_{dd12d}	V