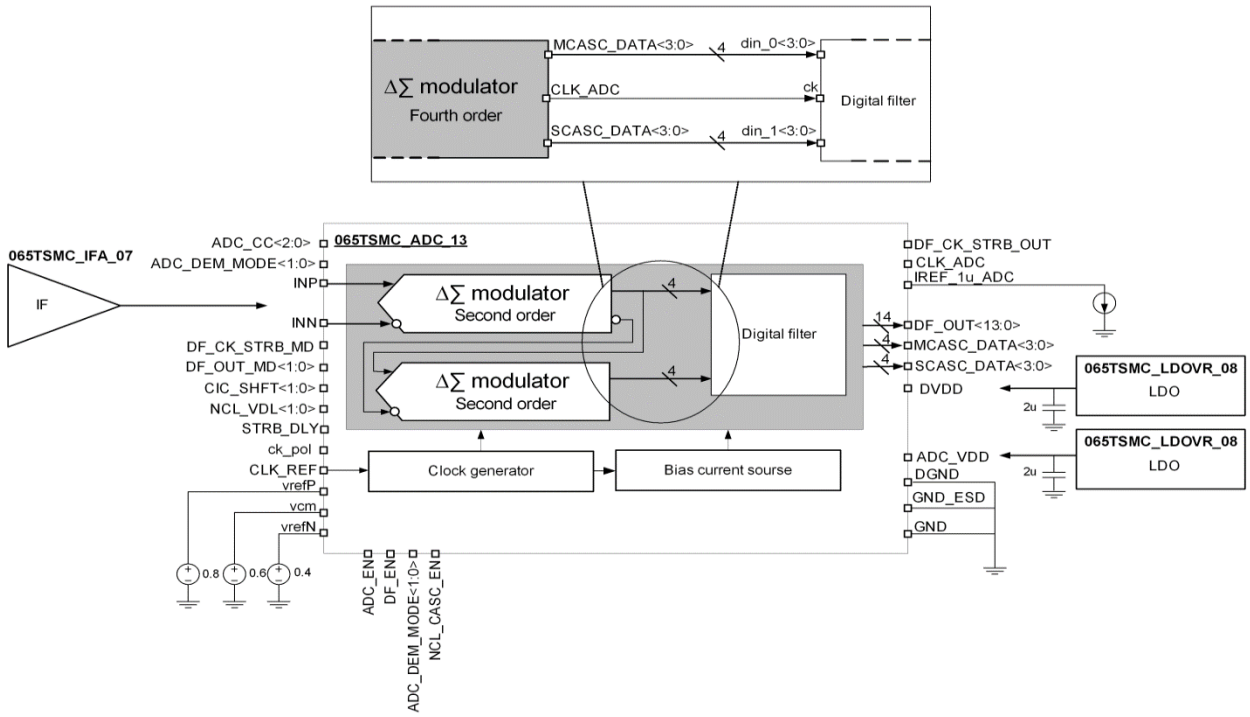
5 MHz 14-bit 1-channel 300 kSPS cascade delta-sigma ADC

OVERVIEW



065TSMC_ADC_13 is fourth order cascade (2-2) delta-sigma ADC with 5-level quantizers in both stages. The block consists of: two delta-sigma modulators second order, coupled in series; clock generator; bias current source; CLA-, DWA-, BiDWA-correction of capacitors mismatch; digital filter.
IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 0.232mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Delta-sigma modulator supply voltage	V_{ADC_VDD}	-	1.14	1.2	1.26	V
Digital filter supply voltage	V_{DVDD}	-	1.14	1.2	1.26	V
Operating temperature	Tj	-	-40	+27	+85	°C
Delta-sigma modulator current consumption	I_{ADC_VDD}	-	90.1	101.7	127	uA
Digital filter current consumption	I_{DVDD}	-	75	100	125	uA
Clock frequency	F_{CLK}	-	-	5	-	MHz
Oversampling ratio	OSR	-	-	16	-	-
Bandwidth	BW	-	-	150	-	kHz
Signal to noise ratio	SNR	BW = 150 kHz	60	67	72	dB
Spurious free dynamic range	SFDR	-	-	78	-	dB
Clock input duty cycle	S	-	45	50	55	%
Clock signal period jitter	T_{JT}	-	-	50	-	pS
Common mode voltage	V_{CM}	-	-	0.6	-	V
Differential reference voltage	V_{REFP}	-	-	0.8	-	V
	V_{REFN}	-	-	0.4	-	
Input logic high level	V_{IH}	For digital inputs	$0.8V_{ADC\_VDD}$	-	V_{ADC_VDD}+0.1	V
Input logic low level	V_{IL}		-0.1	-	$0.2V_{ADC\_VDD}$	V
Output logic high level	V_{OH}	-	-	V_{DVDD}	-	V
Output logic low level	V_{OL}	-	-	0	-	V