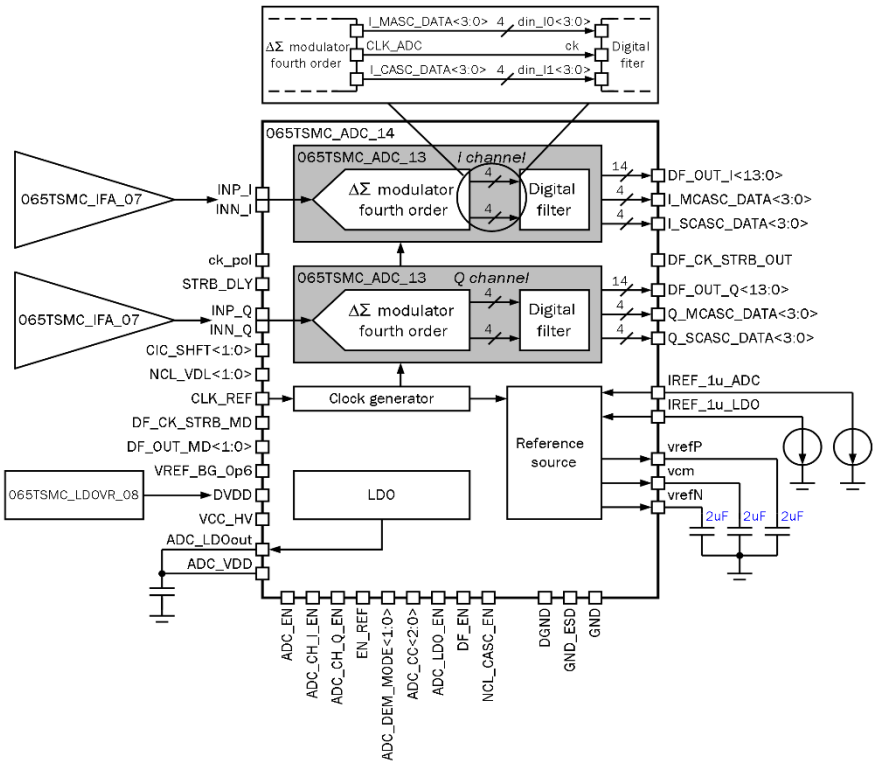
# 5 MHz 14-bit 2-channel 300 kSPS cascade delta-sigma ADC

## OVERVIEW

065TSMC_ADC_14 is fourth order cascade (2-2) delta-sigma ADC with 5-level quantizers in both stages. The block consists of: two delta-sigma modulators second order, coupled in series, in each channel; clock generator; bias current source; voltage reference source; CLA-, DWA-, BiDWA-correction of capacitors' mismatch; digital filter.
IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 0.723mm$^2$.




## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | min | typ. | max | |
| External high supply voltage | $V_{VCC\_HV}$ | - | 1.3 | 2.5 | 3.0 | V |
| Digital filter supply voltage | $V_{DVDD}$ | - | 1.08 | 1.2 | 1.32 | V |
| Delta-sigma modulator output voltage | $V_{ADC\_VDD}$ | - | 1.14 | 1.2 | 1.26 | V |
| Operating temperature | Tj | - | -40 | +27 | +85 | °C |
| Delta-sigma modulator current consumption | $I_{ADC\_VDD}$ | One channel | 0.21 | 0.23 | 0.36 | mA |
| | | Two channels | 0.37 | 0.41 | 0.64 | |
| Reference source current consumption | $I_{VREF}$ | - | 67 | 75 | 220 | uA |
| Digital filter current consumption | $I_{DVDD}$ | - | 150 | 200 | 250 | uA |
| Clock frequency | $F_{CLK}$ | - | - | 5 | - | MHz |
| Oversampling ratio | OSR | - | - | 16 | - | - |
| Bandwidth | BW | - | - | 150 | - | kHz |
| Signal to noise ratio | SNR | BW = 150 kHz | 60 | 67 | 72 | dB |
| Spurious free dynamic range | SFDR | - | - | 78 | - | dB |
| Clock input duty cycle | S | - | 45 | 50 | 55 | % |
| Clock signal period jitter | $T_{JIT}$ | - | - | 50 | - | ps |
| Input differential signal range | $V_{DIF\_p\text{-}p}$ | - | - | 0.64 | - | V |
| Common mode voltage | $V_{CM}$ | - | - | 0.6 | - | V |
| Differential reference voltage | $V_{REFP}$ | - | - | 0.8 | - | V |
| | $V_{REFN}$ | - | - | 0.4 | - | |
| Input logic high level | $V_{IH}$ | For digital inputs | $0.8V_{VCC\_V}$ | - | $V_{VCC\_HV}$+0.1 | V |
| Input logic low level | $V_{IL}$ | | -0.1 | - | $0.2V_{VCC\_HV}$ | V |
| Output logic high level | $V_{OH}$ | - | - | $V_{DVDD}$ | - | V |
| Output logic low level | $V_{OL}$ | - | - | 0 | - | V |