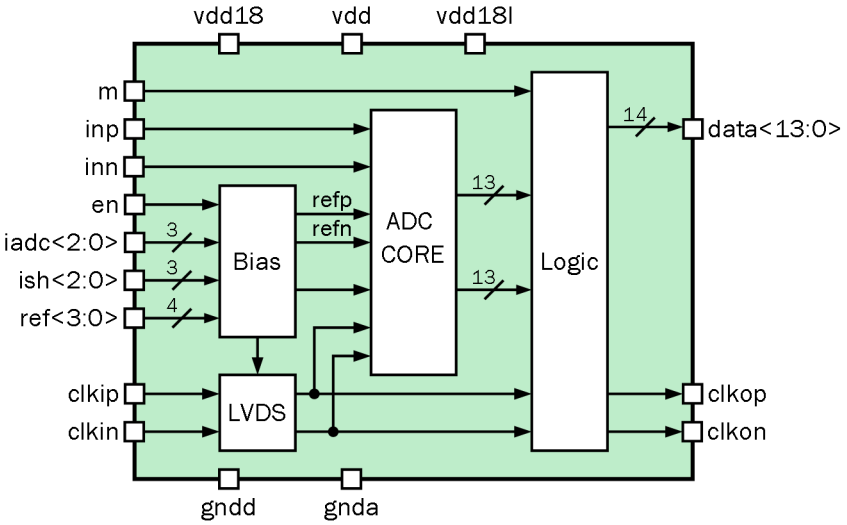
14-bit 1-channel 50 MSPS pipeline ADC

OVERVIEW

090TSMC_ADC_01 has pipelined ADC architecture. This block consists of: bias, LVDS clock receiver, ADC core, output logic correction block. The ADC requires 1.6 ÷ 2 V analog supply and 0.9 ÷ 1.1 V digital supply, there are standby mode which allow to optimize power consumption for system need. Also exist tuning of ADC operating mode by digital correction registers: register **ref<3:0>** specify differential reference range (**refp** and **refn**), register **iadc<2:0>** specify tuning of ADC currents, register **ish<2:0>** specify tuning of sample-and-hold currents, exist possibility to use external voltage source for differential reference **refp** and **refn**.



IP technology: TSMC CMOS 90nm.
IP status: silicon proven.
Area: 0.84mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Analog blocks supply voltage	V_{dd18},V_{dd18l}	-	1.6	1.8	2.0	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Operating temperature range	T_j	-	-60	+27	+125	°C
Current consumption	I_{cc}	-	-	176.8	-	mA
Resolution	N	-	-	14	-	bit
Sampling rate	F_s	-	-	50	-	MSPS
Bandwidth	BW	-	-	25	-	MHz
Stand-by current	I_{stb}	-	-	5	-	uA
Maximum amplitude of input signal	A_{IN}	-	1.02	1.024	1.03	V
Reference voltages for the input signal	V_{REF+}	-	1.31	1.43	1.51	V
	V_{REF-}		0.37	0.41	0.44	V
Analog input voltage range	$A_{IN\ p-p}$	-	-	2	-	V
Input common mode voltage range	U	-	$0.5V_{dd18}$-0.1V	$0.5V_{dd18}$	$0.5V_{dd18}$+0.1V	V
Total harmonic distortion	THD	A_{IN} = 0.9216 V, F_{in} = 1.56 MHz, F_{clk} = 50 MHz	-	-60.5	-	dB
Signal-to-noise ratio	SNR		-	58	-	dB
Spurious-free dynamic range	SFDR		60	62	64	dB
Input logic-level high	V_{IH}	For digital inputs	0.7	-	V_{dd}	V
Input logic-level low	V_{IL}		0	-	0.3	V