12-bit 1-channel 1 to 10 kSPS SAR ADC

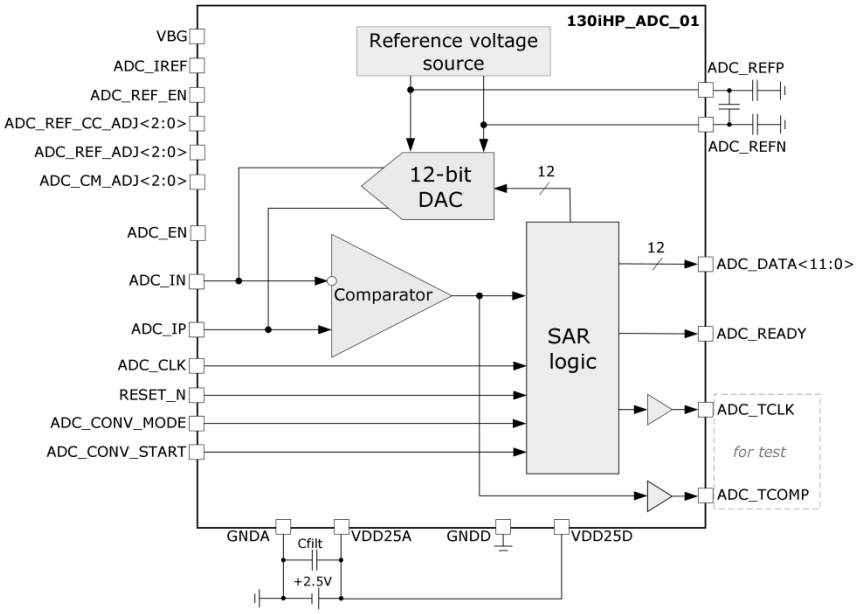
OVERVIEW

130iHP_ADC_01 employs high-performance successive approximation architecture. The ADC operates with sampling rate from 1 to 10 kSPS and input clock from 14 to 140 kHz. The block has differential input and can operate in two modes: single measurement or continuous measurement. The ADC supports standby mode and features low power consumption, compact area.

IP technology: iHP SiGe BiCMOS 0.13um technology.

IP status: silicon proven.

Area: 0.43 mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{DD25A}	-	2.4	2.5	2.6	V
	V_{DD25D}	-	2.4	2.5	2.6	
Operating temperature range	T_j	-	-40	+27	+85	°C
Clock frequency	F_{CLK}	-	14	140	-	kHz
Sample rate	F_S	-	1	10	-	kSPS
Resolution	N	-	-	12	-	bit
Effective number of bits	ENOB	Fs=10kSPS	-	10	-	bit
Spurious-free dynamic range	SFDR	Fs=10kSPS	-	64	-	dB
Differential nonlinearity	DNL	-	-	-	±1	LSB
Reference voltage	V_{REFP}	-	-	1.75	-	V
	V_{REFN}	-	-	0.75	-	
Power consumption	P_{TOTAL}	Standby mode	-	0.5	-	uW
		Active mode @10kSPS	-	1	-	mW
Differential input voltage range	$V_{IN\ p\text{-}p}$	Peak-to-peak differential	-	2	-	V
Clock duty cycle	S	Input clock signal	45	50	55	%
Input high-logic level	V_{IH}	-	V_{DD25D}-0.3	-	V_{DD25D}	V
Input low-logic level	V_{IL}	-	0	-	0.3	
Output high-logic level	V_{OH}	-	V_{DD25D}-0.3	-	V_{DD25D}	V
Output low-logic level	V_{OL}	-	0	-	0.3	