12-bit 800 kSPS cascade delta-sigma ADC

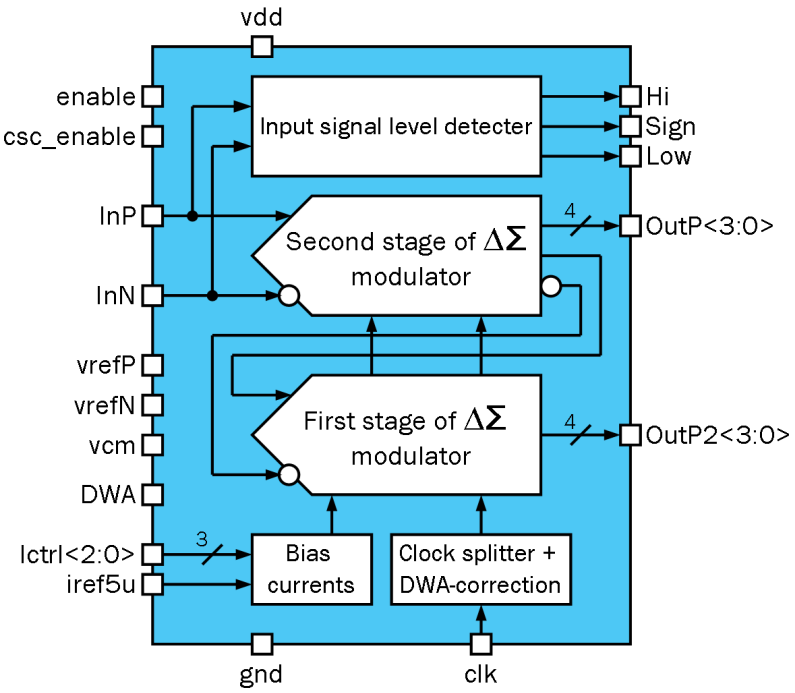
OVERVIEW

The block is third order cascade (2-1) delta-sigma ADC with 5-level quantizers in both stages. The block consists of: two delta-sigma modulators second and first order, coupled in series and combined by noise cancellation logic; clock splitter; block of bias currents, tunable (3-bit control); DWA-correction of capacitors' mismatch; input signal level detection. Output signal is represented in thermometer code at the output of each stage. There is a possibility to disable the second stage of modulator, DWA correction. Tuning of bias current for operational amplifiers with 3-bit control included. Common mode voltage - 0.9 V; recommended values of reference voltages: 0.9 ± 0.4 V; recommended differential input signal amplitude - 0.64 V; allowable duty cycle: 50 ± 5%.

IP technology: TSMC SiGe BiCMOS 180 nm.

IP status: silicon proven.

Area: 0.144mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{dd}	-	1.65	1.8	1.95	V
Reference voltage	V_{ref}	-	0.5	0.9	1.3	V
	Vcm	-	-	0.9	-	
Operating temperature	T_j	-	-45	+27	+85	°C
Resolution	N	-	-	12	-	bit
Clock frequency	F_{clk}	-	8	25	32	MHz
Sampling rate	F_S	-	-	800	-	kSPS
Duty cycle	S	-	45	50	55	%
Oversampling ratio	OSR	-	8	32	40	-
Signal bandwidth	BW	-	400	-	500	kHz
Signal to noise ratio	SNR	F_{clk} = 25 MHz, Fin = 402 kHz, $V_{in\_p\text{-}p}$ = 1.28V	-	82.9	-	dB
		F_{clk} = 25 MHz, Fin = 200 kHz, $V_{in\_p\text{-}p}$ = 1.28V	-	81.7	-	
		F_{clk} = 32 MHz, Fin = 125 kHz, $V_{in\_p\text{-}p}$ = 1.28V	-	77.8	-	
		F_{clk} = 8 MHz, Fin = 125 kHz, $V_{in\_p\text{-}p}$ = 1.28V	-	43.3	-	
Stand-by power	P_{stb}	-	0.014	0.023	0.054	uW
Supply power	P_{supply}	-	2.13	3.19	3.78	mW
Common mode voltage	U	-	-	0.9	-	V
Supply current	I_{supply}	-	1.29	1.77	1.94	mA
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{dd}$	V