

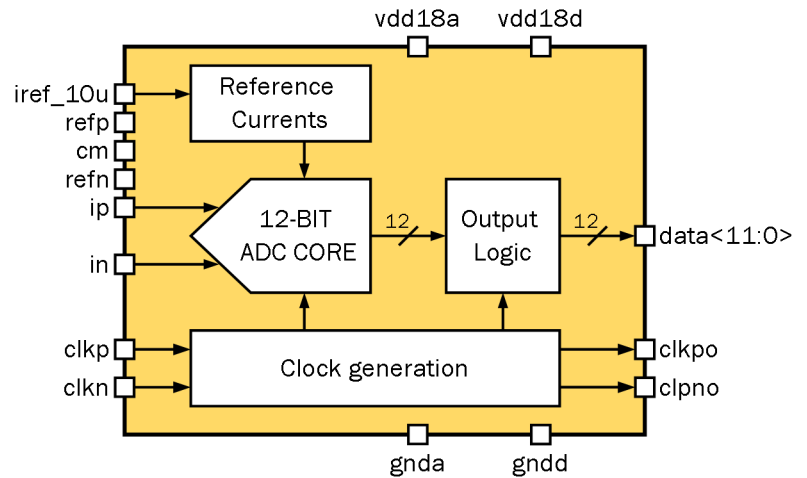
12-bit 1-channel 44/70/90 MSPS pipeline ADC
OVERVIEW

180XFAB_ADC_13 is a low-power high-speed 12-bit ADC that employs high-performance differential pipeline architecture. The ADC consists of a core ADC, output logic, timing generation, reference currents circuits. The ADC requires: $1.7 \div 2$ V analog supply, $1.7 \div 2$ V digital supply, differential reference voltages 1.15 V and 0.65 V, common mode voltage $0.85 \div 1$ V, reference current $9.9 \div 10.1$ uA and differential input clock. The ADC supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.

IP technology: TSMC 180nm CMOS.

IP status: silicon proven.

Area: 1.44mm².


ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units	
			min	typ.	max		
Analog blocks supply voltage	V_{dd18a}	-	1.7	1.8	2	V	
Digital blocks supply voltage	V_{dd18d}	-	1.7	1.8	2	V	
Junction temperature	T_j	-	-40	+27	+85	°C	
Reference current	I_{REF}	-	9.9	10	10.1	uA	
Resolution	N	-	-	12	-	bit	
Sample rate	F_S	-	-	44	90	MHz	
Standby current	I_{STB}	$V_{dd18a} + V_{dd18d}$	-	0.2	-	uA	
Full power bandwidth	BW	-	-	45	-	MHz	
Current consumption	I_{CC}	$V_{dd18a} + V_{dd18d}, F_S = 44$ MHz	-	33	-	mA	
		$V_{dd18a} + V_{dd18d}, F_S = 70$ MHz	-	47	-		
		$V_{dd18a} + V_{dd18d}, F_S = 90$ MHz	-	59	-		
Total power consumption	P_{TOTAL}	$V_{dd18a} + V_{dd18d}, F_S = 44$ MHz	-	59.4	-	mW	
		$V_{dd18a} + V_{dd18d}, F_S = 70$ MHz	-	84.6	-		
		$V_{dd18a} + V_{dd18d}, F_S = 90$ MHz	-	106.2	-		
Input common mode voltage	V_{CM}	-	-	$0.5 V_{dd18a}$	-	V	
Differential reference voltages	V_{REFP}	-	-	$V_{CM} + 0.25$	-	V	
	V_{REFN}	-	-	$V_{CM} - 0.25$	-		
Spurious free dynamic range	SFDR	$F_S = 44$ MHz	$F_{IN} = 1.9$ MHz	70.9	72.7	73.3	dB
			$F_{IN} = 5$ MHz	69.2	72.1	73	
		$F_S = 70$ MHz	$F_{IN} = 1.9$ MHz	70.5	73	75	
			$F_{IN} = 5$ MHz	67	67.5	70	
		$F_S = 90$ MHz	$F_{IN} = 1.9$ MHz	-	74.6	-	
			$F_{IN} = 5$ MHz	-	71.1	-	
Signal-to-noise ratio	SNR	$F_S = 44$ MHz	$F_{IN} = 1.9$ MHz	61.5	61.6	62.2	dB
			$F_{IN} = 5$ MHz	61.4	61.5	62.9	
		$F_S = 70$ MHz	$F_{IN} = 1.9$ MHz	61.7	62.4	62.7	
			$F_{IN} = 5$ MHz	59.3	59.4	59.7	
		$F_S = 90$ MHz	$F_{IN} = 1.9$ MHz	-	61.6	-	
			$F_{IN} = 5$ MHz	-	61.6	-	
Differential nonlinearity	DNL	$F_S = 44$ MHz	$F_{IN} = 1.9$ MHz	-	0.89	-	LSB
		$F_S = 70$ MHz		-	1.09	-	LSB
Integral nonlinearity	INL	$F_S = 44$ MHz	$F_{IN} = 1.9$ MHz	-	2.84	-	LSB
		$F_S = 70$ MHz		-	2.17	-	LSB
Input logic high level	V_{IH}	For digital inputs	$0.7 V_{dd18d}$	-	V_{dd18d}	V	
Input logic low level	V_{IL}		0	-	$0.3 V_{dd18d}$	V	