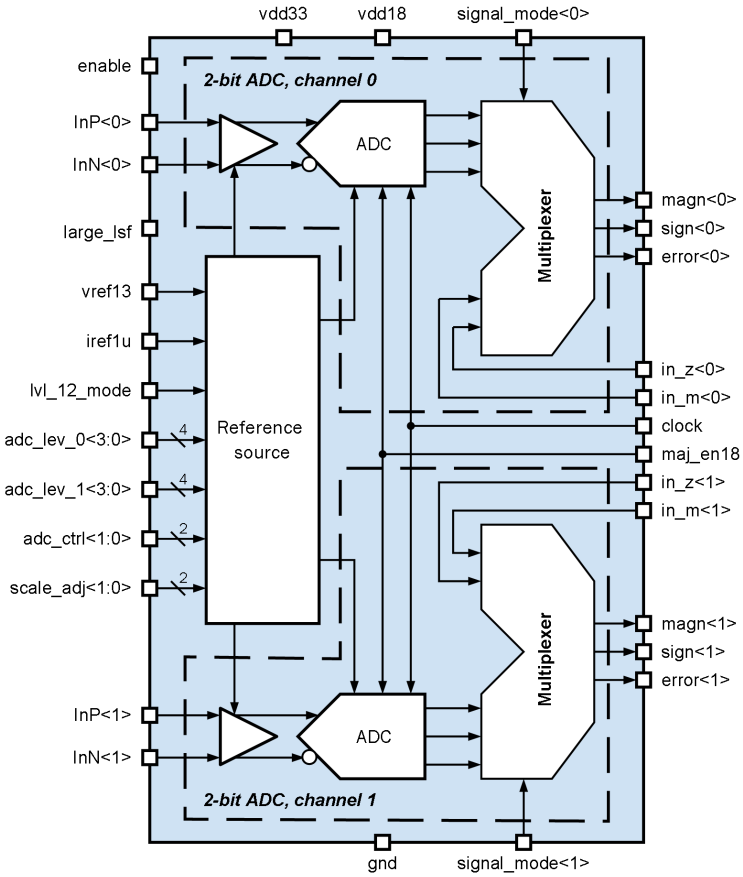
2-bit 2-channel 100 MSPS flash ADC

OVERVIEW

180UMC_ADC_01 is a 2-bit ADC with programmable full scale range of input signal. Low-order bit (sign bit) turns to 1 or 0 with changing of differential input signal's polarity. High-order bit (magnitude bit) turns to 1 when input signal exceeds programmable full scale range of input signal.

The block consists of: reference source; 2 buffers (for each channel); 2 ADCs (for each channel); 2 multiplexers of input signal (for each channel).

Thresholds of full scale are chosen by external 4-bit binary code in a range from 62 mV to 217 mV. The scheme has 2 modes for dividing the ranges of threshold adjustment: "12 levels" mode (step size between values isn't constant) and "16 levels" mode (constant step size between values). There is an opportunity to adjust threshold scale within ±5 mV (the offset is occurring only for magnitude thresholds), moreover full scale is not liable to variation and quantizing step remains unchangeable. Scale adjustment of full scale range affects both ADC channels at the same time.



There is logical error detector in ADC. This detector is forming logical "11" at the error<1:0> output in case of faulty decision.

In order to increase the resistance to false alarms, the scheme applied a triple backup of comparators combined with a majority logical element.

IP technology: UMC CMOS 180 nm.

IP status: silicon proven.

Area: 0.095mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Digital supply voltage	V_{dd18}	-	1.7	1.8	1.9	V
Analog supply voltage	V_{dd33}	-	3.0	3.3	3.6	V
Operating temperature	T_j	-	-45	27	+85	°C
Resolution	N	-	-	2	-	bit
Clock frequency	F_{clk}	-	-	100	-	MHz
Sampling rate	Fs	-	-	100	-	MSPS
Bandwidth	BW	-	25	-	50	MHz
Standby power	P_{st}	-	0.029	23.16	-	uW
Digital blocks supply current	$I_{supply18}$	-	-	2.03	-	uA
Analog blocks supply current	$I_{supply33}$	@two channels	-	3.42	-	uA
Total power	P_{supply}	-	-	14.94	-	mW
DC level of input signal	U	-	1.5	1.7	1.9	V
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd18}$	-	$V_{dd18}+0.25$	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{dd18}$	V