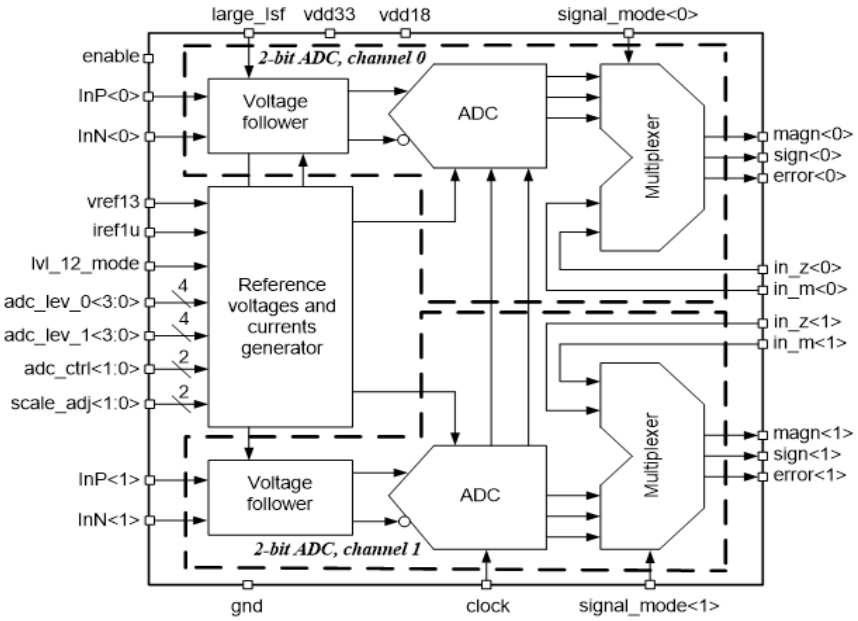
2-bit 2-channel 50 MSPS flash ADC

OVERVIEW

180UMC_ADC_02 is a 2-bit ADC with programmable threshold. Least significant bit, calling sign bit, turns to 1 or 0 with changing of differential input signal's polarity. Most significant bit, calling magnitude bit, turns to 1 if there is an excess of the threshold by differential input signal.



The block consists of reference voltages and currents generator, 2 voltage followers, 2 ADCs (for each channel) and multiplexers of input signal.

Thresholds are chosen by external 4-bit binary code in range from 60 mV to 220 mV. Threshold's step equals 10 mV. There are two modes to define the threshold: «12 levels» mode and «16 levels» mode. Shifting between these modes is adjusted by logical level at lvl_12_mode input: logical "1" for «12 levels» mode; logical "0" for «16 levels» mode. There is a possibility to adjust the dc level of thresholds' scale within 10 mV, wherein quantizing step remains unchangeable. Scale adjustment implemented by binary code at input scale_adj. Scale adjustment affects both channels at the same time.

There is logical error detector in ADC. In case of appearance one of faulty decisions logical level at the error output of corresponding channel. The faulty decisions are:

- Simultaneous signal of negative sign and upper threshold crossing
- Simultaneous signal of positive sign and lower threshold crossing
- Simultaneous signal of both upper and lower thresholds crossing

IP technology: UMC CMOS 180 nm.

IP status: silicon proven.

Area: 0.053mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Digital supply voltage	V_{dd18}	-	1.7	1.8	1.9	V
Analog supply voltage	V_{dd33}	-	3.0	3.3	3.6	V
Operating temperature	T_j	-	-45	27	+85	°C
Resolution	N	-	-	2	-	bit
Clock frequency	F_{clk}	-	-	50	-	MHz
Sampling rate	F_S	-	-	50	-	MSPS
Bandwidth	BW	-	25	-	50	MHz
Standby power	P_{st}	-	0.016	29.1	-	uW
Digital blocks supply current	$I_{supply18}$	-	-	0.7	-	mA
Analog blocks supply current	$I_{supply33}$	@ two channels	-	1.4	-	mA
Total power	P_{total}	-	-	6.93	-	mW
DC level of input signal	U	-	1.5	1.7	1.9	V
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd18}$	-	$V_{dd18}+0.25$	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{dd18}$	V