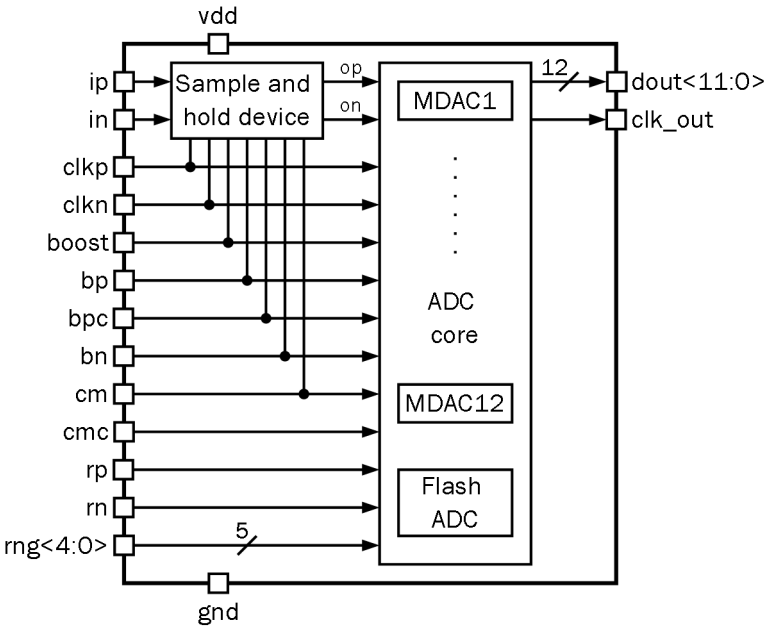
12-bit 1-channel 10 to 100 MSPS pipeline ADC

OVERVIEW

250iHP_ADC_02 is a low-power high-speed 12-bit ADC that employs high-performance differential pipeline architecture. The ADC consists of a sample and hold device, a core ADC and block of comparators. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 0.75 V and differential input clock. The block supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.
IP technology: iHP SiGe BiCMOS 0.25 um.
IP status: silicon proven.
Area: 1.14mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{dd}	-	2.25	2.5	2.75	V
Operating temperature range	T_j	-	-60	+27	+125	°C
Resolution	N	-	-	12	-	Bit
Maximum input amplitude	A_{IN}	-	-	0.5	-	V
Bandwidth	BW	-	5	-	50	MHz
Sampling rate	F_S	-	10	-	100	MSPS
Current consumption	I_{CC}	-	-	60	-	mA
Standby current	I_{STB}	-	-	60	-	uA
Input reference voltage	V_{REF+}	-	-	1.5	-	V
	V_{REF-}		-	1	-	V
Peak-to-peak differential input voltage	$A_{IN\ p-p}$	-	-	1	-	V
DC operating point	U	-	$0.5V_{dd}$ - 0.1	$0.5V_{dd}$	$0.5V_{dd}$ + 0.1	V
Signal - noise ratio	SNR	A_{IN} = 0.45V, F_{IN} = 10.7MHz, F_{CLK} = 50MHz	-	61	-	dB
Spurious-free dynamic range	SFDR		56	62	64	dB
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	0.3	V