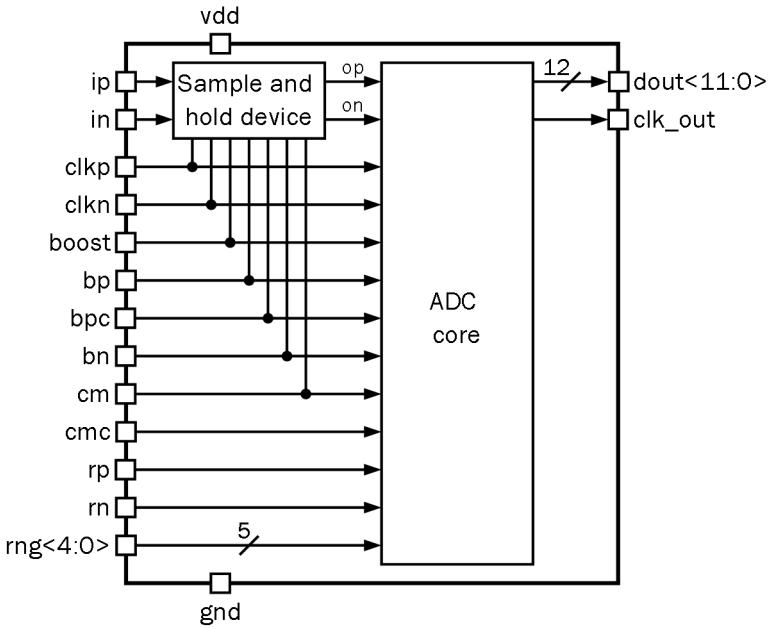
12-bit 1-channel 15 - 25 MSPS pipeline ADC

OVERVIEW

250iHP_ADC_03 is a low-power high-speed 12-bit ADC that employs high-performance differential pipeline architecture. The block consists of a sample and hold device, a core ADC and block of comparators. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 1.25 V and differential input clock. The ADC supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.
IP technology: iHP SiGe BiCMOS 0.25 um.
IP status: silicon proven.
Area: 0.78mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{dd}	-	2.25	2.5	2.75	V
Operating temperature range	T	-	-60	+27	+125	°C
Resolution	N	-	-	12	-	bit
Current consumption	I_{cc}	-	-	50	-	mA
Standby current	I_{st}	-	-	60	-	uA
Bandwidth	B	-	7.5	10.0	12.5	MHz
Clock frequency	F_{CLK}	-	15	20	25	MHz
Sampling rate	F_S	-	15	20	25	MSPS
Input reference voltage	V_{rp}	-	-	1.5	-	V
	V_{rn}		-	1	-	V
Peak-to-peak differential input voltage	$A_{IN\ p\text{-}p}$	-	-	1	-	V
DC operating point	U	-	$0.5V_{dd}$-0.1V	$0.5V_{dd}$	$0.5V_{dd}$+0.1V	V
Signal-noise ratio	SNR	Input amplitude $0.9*A_{IN}$, F_{IN} = 1.5MHz, F_{CLK} = 20MHz	-	61	-	dB
Spurious-free dynamic range	SFDR		56	62	64	dB
Effective number of bits	ENOB	From SFDR	-	10	-	bit
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V