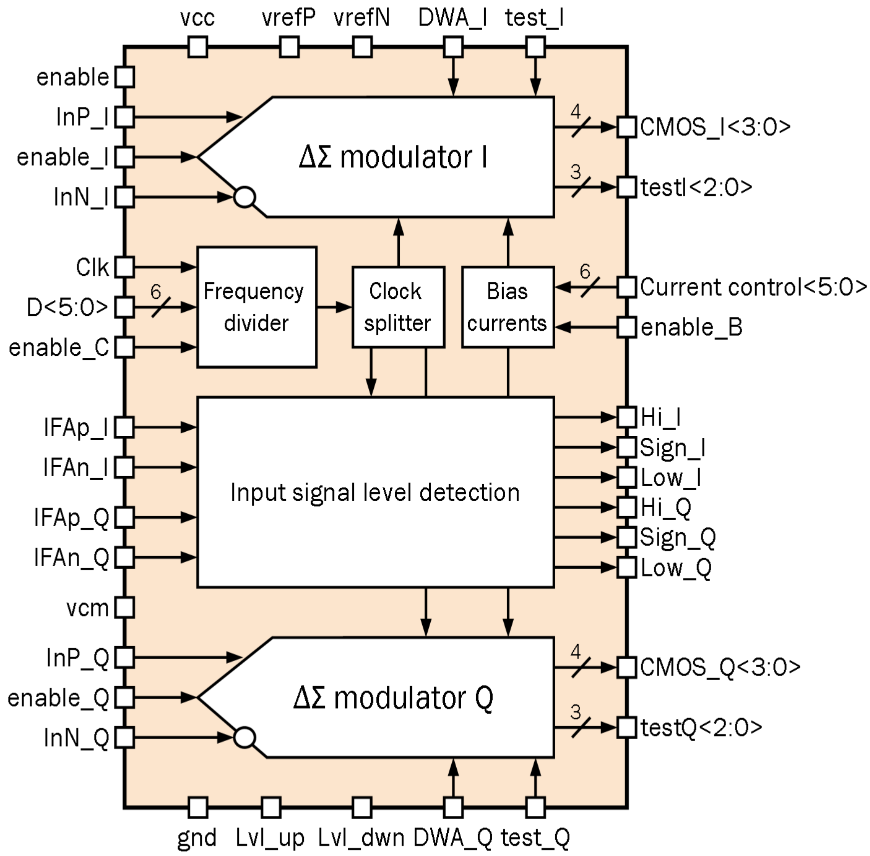
12-bit 2-channel 0.5 to 33 MSPS delta-sigma ADC

OVERVIEW



250iHP_ADC_04 is second order delta-sigma ADC with 5-level quantizer. The block consists of: two integrating cascades based on switch capacitors technique (treats both channels); 5-level flash-ADC (treats both channels); tunable (6-bit control) clock signal frequency divider; clock splitter; block of bias currents, tunable (6-bit control); data-weighted averaging (DWA) correction of capacitors mismatch (treats both channels); input signal level detection. Output signal is represented in "thermometer" code. There is a possibility to disable of each channel, frequency divider, block of bias currents, DWA correction. There is an in-built output from frequency divider for clocking digital filters. Input DC level is 0.9 V; recommended voltage levels for references are 0.9 ± 0.4 V; recommended input signal differential amplitude is 0.64 V; allowable deviation of clock duty cycle: 50 ± 5%.

IP technology: iHP SiGe BiCMOS 0.25 um.

IP status: silicon proven.

Area: 0.3mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{cc}	-	1.7	1.8	1.9	V
Operating temperature	T_j	-	-45	+27	+85	°C
Current consumption	I_{cc}	One channel @BW = 8 kHz	0.232	0.239	0.272	mA
		One channel @BW = 512 kHz	4.455	4.549	4.676	mA
Standby current	I_{STB}	-	0.68	1.86	4.01	uA
Resolution	N	-	-	12	-	bit
Oversampling ratio	OSR	-	32	-	-	-
Sampling rate	F_S	-	0.5	-	33	MSPS
Bandwidth	BW	-	8	128	512	kHz
Differential peak-to-peak input voltage	$V_{in\_diff\ p\text{-}p}$	-	-	1.6	-	V
Signal-to-noise ratio	SNR	With an amplitude closed to the maximum	58	61	63	dB
Spurious free dynamic range	SFDR	-	55	63	65	dB
Common mode voltage	U	-	-	0.9	-	V
Duty cycle	DC	-	45	50	55	%
Input high level voltage	V_{IH}	For digital inputs	$0.7*V_{cc}$	-	$V_{cc}+0.25$	V
Input low level voltage	V_{IL}	For digital inputs	-0.25	-	$0.3*V_{cc}$	V