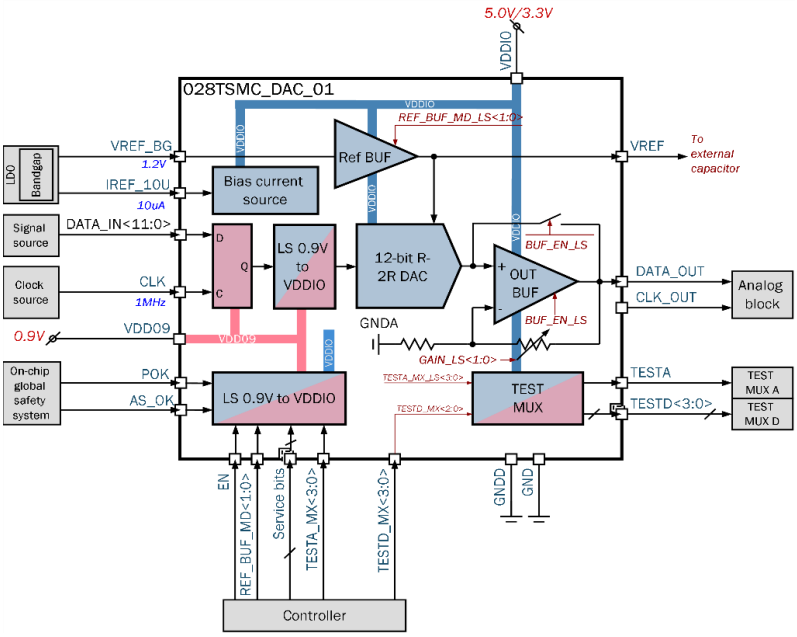
12-bit 1-channel up to 1 MSPS R/2R DAC

OVERVIEW

028TSMC_DAC_01 is a 12-bit digital to analog converter (DAC) with sample rates up to 1 MSPS. The block contains four main blocks: reference voltage source, bias voltage source, DAC core and control digital module. DAC core consist of the R/2R matrix and output operational class AB amplifier. The DAC operates directly from VDDIO/VDD33 supplies which are filtered analog supply pins of the chip. Analog voltage references can be generated from internal buffer or supplied externally.
IP technology: TSMC 28nm eFlash.
IP status: pre-silicon verification.
Silicon area: 0.091mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{DDIO}	Option 5V		4.5	5	5.5	V
		Option 3.3V		2.97	3.3	3.63	V
Digital supply voltage	V_{DD09}	-		0.855	0.9	0.945	V
Temperature range	T_j	-		-40	+85	+150	°C
Input clock frequency	F_{CLK}	-		0.8	1	1.2	MHz
Input clock frequency jitter	J_{CLK}	@1MHz		-	-	10	ps
Load resistance	R_{LOAD}	-		-	50	-	kOhm
Load capacity	C_{LOAD}	-		-	10	-	pF
Resolution	N	-		-	12	-	bit
Output impedance	R_{OUT}	-		-	-	30	kOhm
Output frequency bandwidth	BW	-		-	-	20	kHz
Output signal amplitude	A_{OUT}	@V_{DDIO} = 5.0V		0	-	5.5	V
		@V_{DDIO} = 3.3V		0	-	3.3	
Sampling rate	SR	-		-	-	1	MSPS
Current consumption	I_{CC}	@V_{DDIO}, F_S=1MSPS	Option 5V	-	0.7	0.9	mA
			Option 3.3V	-	0.6	0.9	
		@V_{DD09}, F_S=1MSPS		-	0.2	3.3	uA
Shutdown current consumption	I_{STB}	Option with V_{DDIO}=5V	@V_{DDIO}	-	2.3	277	nA
			@V_{DD09}	-	38	20200	
		Option with V_{DDIO}=3.3V	@V_{DDIO}	-	1.3	277	nA
			@V_{DD09}	-	28.4	20200	
Differential nonlinearity	DNL	Reduced code range from 128 to 3967		-	±0.2	±0.3	LSB
Integral nonlinearity	INL	Reduced code range from 128 to 3967	@V_{DDIO}=5.0V	-	±0.4	±0.7	LSB
			@V_{DDIO}=3.3V	-	±0.3	±0.7	
Spurious-Free Dynamic Range	SFDR	F_{out} =3.9KHz and bandwith 20kHz	@V_{DDIO}=5.0V	79.8	83.4	84.9	dB
			@V_{DDIO}=3.3V		82.2		
Signal to noise and distortion ratio	SINAD	F_{out} =3.9Khz and BW = 20kHz	@V_{DDIO}=5.0V	82.2	81.3	82.1	dB
			@V_{DDIO}=3.3V		83.4		
Effective number of bits	ENOB	F_{out} =3.9KHz and BW = 20kHz	@V_{DDIO}=5.0V	12.7	13.2	13.3	dB
			@V_{DDIO}=3.3V		13.0		
Offset error	OE	-		-	±9	-	LSB
Gain error	GE	-		-	±12	-	LSB