12-bit 50 - 500 MSPS current steering IQ DAC

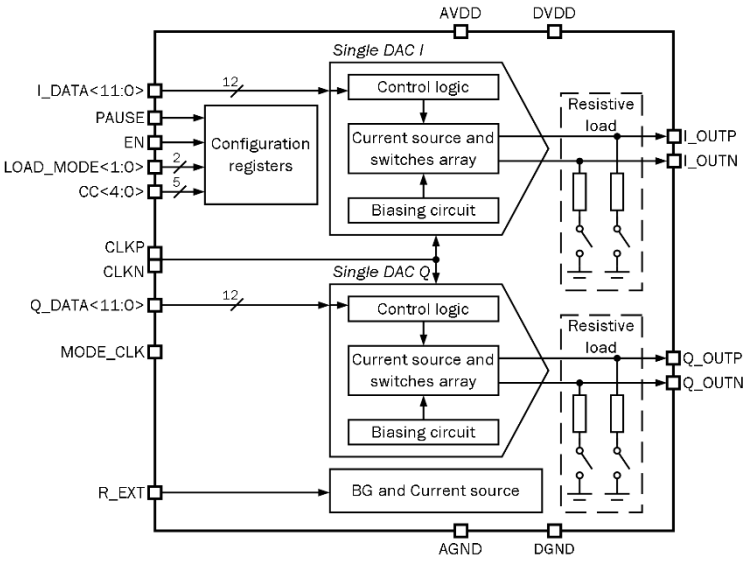
OVERVIEW

065TSMC_DAC_01 employs a high-performance current steering architecture and provides optional differential current output or differential voltage output. The bandgap and current source included to provide a complete DAC. The DAC can be configured to adjust full-scale output range. The DAC uses segmentation architecture combined with Q^2 random walk algorithm to achieve excellent dynamic and static performance, wide output bandwidth. An internal resistive load together with current source is used to set differential voltage output, which independent from process, supply and temperature.

IP technology: TSMC CMOS 65nm.

IP status: pre-silicon verification.

Area: 0.47mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{AVDD}	-		2.25	2.5	2.75	V
Digital supply voltage	V_{DVDD}	-		1.08	1.2	1.32	V
Operating temperature range	T_j	-		-40	27	+85	°C
Current consumption	I_{CC}	Normal mode, $A_{IOUT\ p\text{-}p}$=20.48mA, F_S=500MSPS	@V_{AVDD}	-	41.6	-	mA
			@V_{DVDD}		7.6		
	I_{STB}	Standby mode		-	3	-	uA
Total power consumption	P_{CP}	Pause mode, $A_{IOUT\ p\text{-}p}$=20.48mA, F_S =500MSPS		-	103	-	mW
Resolution	N	-		-	12	-	bit
Differential nonlinearity	DNL	-		-	±0.2	-	LSB
Integral nonlinearity	INL	-		-	±0.5	-	LSB
Offset error	OE	-		-	0.1	-	LSB
Gain error	GE	-		-	0.3	-	LSB
Output resistance	R_{OUT}	-		-	200	-	kOhm
Sampling rate	F_S	-		50	-	500	MSPS
Duty cycle	S	-		45	50	55	%
Signal-to-noise ratio	SNR	F_S=100MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	72.6	-	dB
			Fin = 20 MHz	-	72.4	-	dB
		F_S=250MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	73.5	-	dB
			Fin = 20 MHz	-	73.9	-	dB
			Fin = 150 MHz	-	71.2	-	dB
		F_S=500MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	73.1	-	dB
			Fin = 20 MHz	-	72.7	-	dB
			Fin = 150 MHz	-	71.7	-	dB
Spurious-free dynamic range	SFDR	F_S=100MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	83.5	-	dB
			Fin = 20 MHz	-	68.9	-	dB
		F_S=250MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	81.7	-	dB
			Fin = 20 MHz	-	77.3	-	dB
			Fin = 150 MHz	-	64.3	-	dB
		F_S=500MSPS, $A_{VOUT\ p\text{-}p}$ = 1.024V	Fin = 10 MHz	-	81.3	-	dB
			Fin = 20 MHz	-	77.5	-	dB
			Fin = 150 MHz	-	56.3	-	dB
Input high-logic level	V_{IH}	-		$0.7V_{dvdd}$	-	-	V
Input low-logic level	V_{IL}	-		-	-	$0.3V_{dvdd}$	V