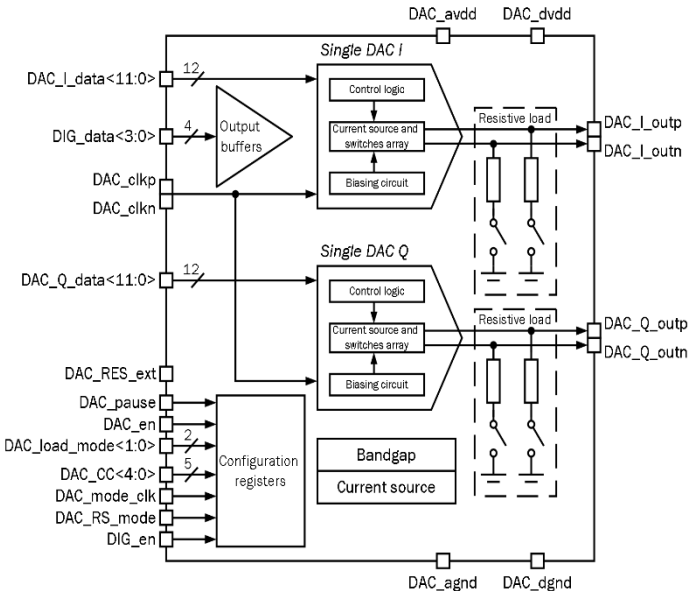
12-bit 50 - 140 MSPS current steering IQ DAC

OVERVIEW

065TSMC_DAC_01 employs a high-performance current steering architecture and provides optional differential current output or differential voltage output. The bandgap and current source are included to provide a complete DAC. The block can be configured to adjust full-scale output range. The DAC uses segmentation architecture combined with Q^2 random walk algorithm to achieve excellent dynamic and static performance, wide output bandwidth. An internal resistive load together with current source is used to set differential voltage output, which independent from process, supply and temperature. LVDS transmitter, output buffers and IO PADs are included.
IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 0.66mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{avdd}	Pin DAC_avdd		2.25	2.5	2.75	V
Digital supply voltage	V_{dvdd}	Pin DAC_dvdd		1.08	1.2	1.32	V
Operating temperature range	T_j	-		-40	+27	+85	°C
Analog current consumption	I_{ACN}	$A_{IOUT\ p-p}$=20.48mA, F_S = 140MSPS	Normal mode	-	40.4	-	mA
	I_{ACP}		Pause mode	-	40	-	mA
Digital current consumption	I_{DCN}	$A_{IOUT\ p-p}$= 20.48mA, F_S = 140MSPS	Normal mode	-	7.6*	-	mA
	I_{DCP}		Pause mode	-	60*	-	uA
Current consumption	I_{STB}	Standby mode		-	3*	-	uA
Resolution	N	-		-	12	-	bit
Differential nonlinearity	DNL	-		-	±0.2*	-	LSB
Integral nonlinearity	INL	-		-	±0.5*	-	LSB
Offset error	OE	-		-	±0.1*	-	LSB
Gain error	GE	-		-	±0.3*	-	LSB
Differential full-scale output current range	$A_{IOUT\ p-p}$	External R_{LOAD} or transformer	Minimum range	-	2.6*	-	mA
			Maximum range	-	22.4*	-	mA
Differential full-scale output voltage range	$A_{VOUT\ p-p}$	Internal R_{LOAD}=50Ohm	Minimum range	-	0.26*	-	V
			Maximum range	-	2.24*	-	V
		Internal R_{LOAD}=100Ohm	Minimum range	-	0.13*	-	V
			Maximum range	-	1.12*	-	V
Output resistance	R_{OUT}	-		-	200*	-	kOhm
Sampling rate	F_S	-		50	-	140	MSPS
Duty cycle	S	-		45	50	55	%
Spurious-free dynamic range	SFDR	F_S = 50MSPS, $A_{VOUT\ p-p}$ = 1.28V	Fin= 5MHz	64.4	68.1	72.9	dB
			Fin= 10MHz	59.0	65.5	70.1	dB
			Fin= 20MHz	53.0	61.1	64.7	dB
		F_S = 100MSPS, $A_{VOUT\ p-p}$ = 1.28V	Fin= 5MHz	64.8	69.5	73.8	dB
			Fin= 10MHz	63.7	68.3	72.6	dB
			Fin= 20MHz	62.3	64.4	65.4	dB
		F_S = 140MSPS, $A_{VOUT\ p-p}$ = 1.28V	Fin= 5MHz	65.0	70.7	73.9	dB
			Fin= 10MHz	63.3	69.2	74.0	dB
			Fin= 20MHz	60.5	62.7	65.5	dB
Input logic-level high	V_{IH}	-		0.7*V_{dvdd}	-	V_{dvdd}	V
Input logic-level low	V_{IL}	-		0	-	0.3*V_{dvdd}	V

*-according to modeling