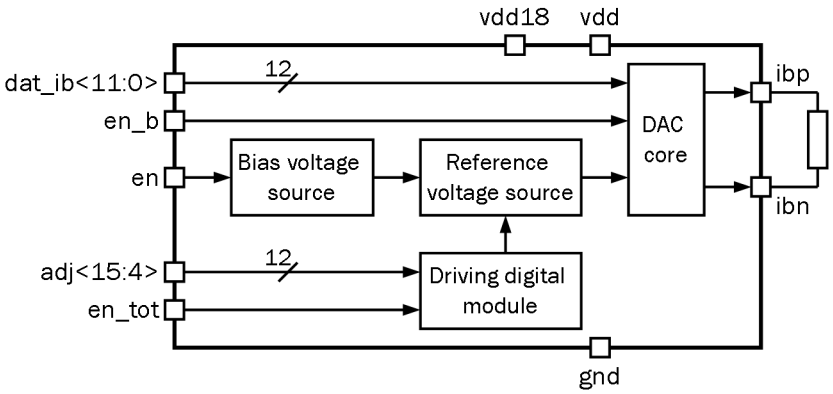
12-bit 1-channel up to 1 MSPS R/2R ADC

OVERVIEW

090TSMC_DAC_02 is a 12-bit 1-channel R/2R DAC with sampling rate up to 1 MSPS. The DAC contains four main blocks: reference voltage source, bias voltage source, DAC core and control digital module. DAC core consist of the R/2R matrix and output operational class AB amplifier. Digital control register **adj<15:4>** sets optimal mode. It corrects output buffers current, common mode and output signal swing.



DAC requires 1.62 ÷ 1.98 V (port V_{dd18}) analog supply voltage and 0.9 ÷ 1.1 V (port V_{dd}) digital supply voltage.
IP technology: TSMC CMOS 90nm.
IP status: silicon proven.
Area: 0.246mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Analog blocks supply voltage	V_{dd18}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Operating temperature range	T_j	-	-60	+27	+125	°C
Resolution	N	-	-	12	-	bit
Resistive load	R_{LOAD}	-	5	-	-	kOhm
Sampling rate	F_S	-	-	1	-	MSPS
Current consumption	I_{CC}	@F_S = 1MSPS	0.47	0.88	1.95	mA
Standby current	I_{STB}	-	-	180	-	nA
Power consumption	P_{CC}	-	0.76	1.53	3.86	mW
Differential output voltage range	V_{REF}	-	1	1	2	V
Common mode of output signal	V_{CM}	-	0.68	1	1.3	V
Maximum differential nonlinearity	DNL	F_S = 1MSPS, adjust registers value: adj<15:4> = "100000000100"	±0.5	±0.7	±0.9	LSB
Maximal integrated nonlinearity	INL		±0.9	±1.2	±1.5	LSB
Offset error	OE		-	±0.9	±8	LSB
Gain error	GE		-	±0.2	±0.9	LSB
Time setup	t_{set}		276	278	279	ns
Input high-logic level	V_{IH}	-	0.7*V_{dd}	-	V_{dd}	V
Input low-logic level	V_{IL}		-	-	0.3*V_{dd}	V