12-bit 16-channel 1 MSPS R/2R DAC

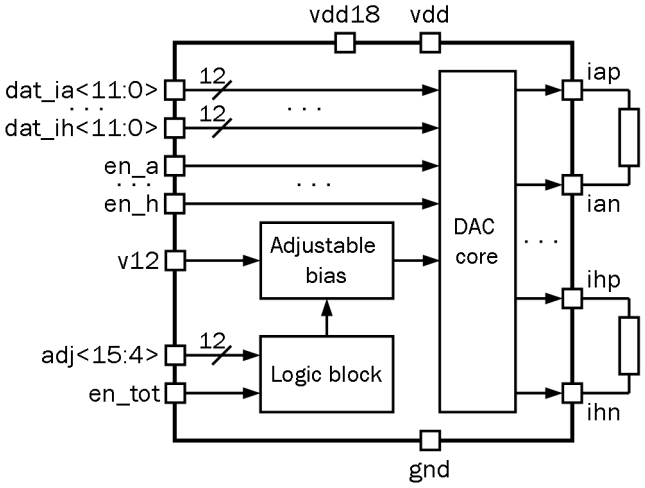
OVERVIEW

090TSMC_DAC_06 is a 16-channels 12-bit R/2R DAC contains a three principal blocks: adjustable bias, DAC core and logic block. DAC core consist of 16 identical R/2R DAC, each of which include differential R/2R ladder and output operational amplifier AB class. There is a possibility to turn off each output channels and whole scheme Digital control register adj<15:4> sets optimal mode by reducing current consumption. It corrects output buffers current, common mode and swing output signal. DAC requires 1.62 ÷ 1.98 V (port V_{dd18}) analog supply and 0.9 ÷ 1.1 B (port V_{dd}) digital supply.

IP technology: TSMC CMOS 90nm.

IP status: silicon proven.

Area: 1.76mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Analog blocks supply voltage	V_{dd18}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Operating temperature range	T_j	-	-60	27	+125	°C
Reference voltage	V_{ref}	-	1.08	1.2	1.32	V
Resolution	N	-	-	12	-	bit
Clock frequency	F_{clk}	-	-	1	-	MHz
Sampling rate	F_s	-	-	1	-	MSPS
Standby current	I_{st}	-	-	650	-	nA
Power consumption	P_{cn}	-	4.34	11.9	43.04	mW
Current consumption	I_{cn}	-	2.68	6.6	21.74	mA
Differential output voltage range	V_{dref}	-	1.04	1.04	2.0	V
Common mode of output signal	V_{cmout}	-	0.68	1.0	1.3	V
Maximum differential nonlinearity	DNL	F_{clk}=1 MHz, adjust registers value: adj<15:4> = “100000000100”	-	±0.74	±0.93	LSB
Maximal integrated nonlinearity	INL		-	±1.20	±1.48	LSB
Offset error	OE		-	±0.88	±8.0	LSB
Gain error	GE		-	±0.17	±0.89	LSB
Time setup	t_{set}		276	278	279	ns
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}	V
Input low-logic level	V_{IL}		-	-	0.3	V