180TSMC_DAC_07

## 12-bit 2-channel up to 50 MSPS current steering DAC

## OVERVIEW

180TSMC_DAC_07 is a 12 -bit 50 MSPS dual current steering DAC contains two DAC cores, reference current, bandgap, configuration register. Core DAC is based on current steering architecture and contains control logic, current source, switches array and reference voltage. There are two operation modes: with external reference current and internal reference current, which independent from voltage supply, temperature and dependent from process variations of resistor. DAC has a feature of adjusting output current. A segmented DAC architecture and $\mathrm{Q}^{2}$ random walk algorithm are used. DAC requires: $3.0 \div 3.6 \mathrm{~V}$ analog supply, $3.0 \div 3.6 \mathrm{~V}$ digital supply, differential input clock signal with duty cycle $45 \div 55 \%$. 12-bit 50 MSPS dual current steering DAC supports standby mode.


IP technology: TSMC CMOS 180 nm .
IP status: silicon proven.
Area: $0.68 \mathrm{~mm}^{2}$.

## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions |  | Value |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | min | typ. | max |  |
| Analog blocks supply voltage | $\mathrm{V}_{\text {dd_a }}$ | Pin DAC_avdd |  | 3.0 | 3.3 | 3.6 | V |
| Digital blocks supply voltage | $\mathrm{V}_{\text {dd_d }}$ | Pin DAC_dvdd |  | 3.0 | 3.3 | 3.6 | V |
| Operating temperature range | $\mathrm{T}_{\mathrm{j}}$ | - |  | -40 | +27 | +125 | ${ }^{\circ} \mathrm{C}$ |
| Reference current | $\mathrm{I}_{\text {ref }}$ | - |  | 9.8 | 10 | 10.2 | uA |
| Output current range | Iout p-p | DAC_CC $<3: 0>=$ " 0000 " |  | - | 5 | - | mA |
|  |  | DAC_CC $<3: 0>=$ " 0101 " |  | - | 10 | - | mA |
|  |  | DAC_CC $<3: 0>=$ "1111" |  | - | 20 | - | mA |
| Resolution | N | - |  | - | 12 | - | bit |
| Duty cycle | S | - |  | 45 | 50 | 55 | \% |
| Sampling rate | $\mathrm{F}_{S}$ | - |  | 0 | - | 50 | MSPS |
| Standby current | $\mathrm{I}_{\text {STB }}$ | - |  | - | 100 | - | nA |
| Power dissipation | $\mathrm{P}_{\mathrm{cn}}$ | DAC_CC $<3: 0>=$ " 0101 " |  | - | 75.24 | - | mW |
| Current consumption | $\mathrm{I}_{\mathrm{cn}}$ | DAC_CC $<3: 0>=$ "0101" |  | - | 22.8 | - | mA |
| Spurious-free dynamic range | SFDR | $\begin{aligned} & \text { Fs = } 50 \mathrm{MSPS}, \\ & \text { DAC_CC }<3: 0>=" 0101 " \end{aligned}$ | $\mathrm{F}_{\text {in }}=1.575 \mathrm{MHz}$ | - | 88 | - | dB |
|  |  |  | $\mathrm{F}_{\text {in }}=11.513 \mathrm{MHz}$ | - | 89 | - | dB |
| Signal-to-noise ratio | SNR |  | $\mathrm{F}_{\text {in }}=1.575 \mathrm{MHz}$ | - | 70 | - | dB |
|  |  |  | $\mathrm{F}_{\text {in }}=11.513 \mathrm{MHz}$ | - | 70 | - | dB |
| Signal-to-noise anddistortion ratio | SINAD |  | $\mathrm{F}_{\text {in }}=1.575 \mathrm{MHz}$ | - | 70 | - | dB |
|  |  |  | $\mathrm{F}_{\text {in }}=11.513 \mathrm{MHz}$ | - | 70 | - | dB |
| Input high-logic level | $\mathrm{V}_{\text {IH }}$ | - |  | $0.7 \mathrm{~V}_{\text {dd d }}$ | - | - | V |
| Input low-logic level | $\mathrm{V}_{\text {IL }}$ | - |  | - | - | $0.3 \mathrm{~V}_{\text {dd_d }}$ | V |

