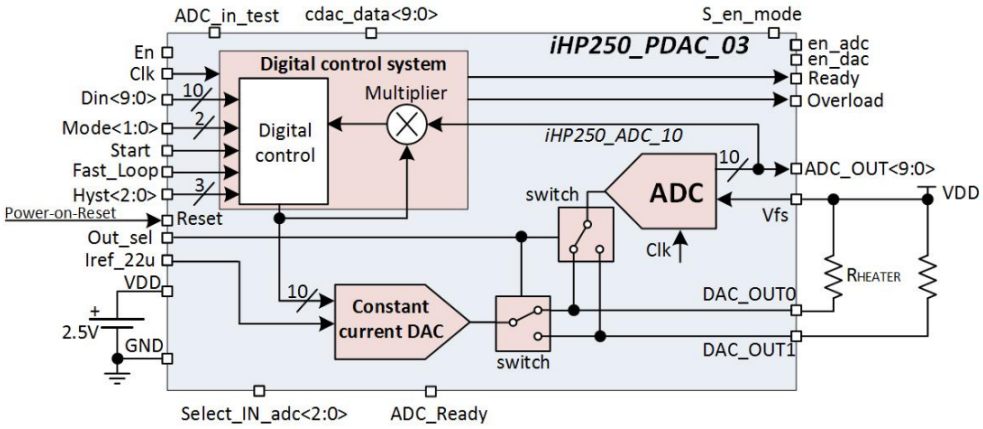
10-bit 1-channel constant power DAC

OVERVIEW



10-bit constant power DAC employs a current steering DAC architecture with control loop, which adjusts DAC input code to keep power dissipated in terminator constant. The block is easy to configure and operate, combining good accuracy and linearity. Several operation modes are available: constant power DAC, current DAC with output voltage monitoring, current DAC (manual mode), low-speed ADC. Output DAC current could be fed to one of two DAC outputs (DAC_OUT0 or DAC_OUT1) depending on Out_sel input.

IP technology: iHP SiGe BiCMOS 0.25 um.

IP status: pre-silicon verification.

Area: 0.34 mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{DD}	-	2.375	2.5	2.625	V
Operating temperature range	T_J	-	0	+50	+100	°C
DAC resolution	N_{DAC}	-	-	10	-	bit
ADC resolution	N_{ADC}	-	-	10	-	bit
Input reference current	I_{REF}	-	-	20	-	uA
Full-scale output current	I_{OUT}	Mode = "01"	-	22	-	mA
Full-scale output power	P_{OUT}	Mode = "10"	-	-	56.3	mW
Power adjustment step	P_{step}	Mode = "11"	55	-	-	uW
CDAC differential nonlinearity	DNL	Mode = "11"	-	0.6	-	LSB
CDAC integral nonlinearity	INL	RHEATER=120Ohm	-	<1	-	LSB
Output resistance	R_{OUT}	VDAC_OUT > 0.3V	-	100	-	kOhm
Targeted load resistance	R_{LOAD}	VDAC_OUT > 0.3V	-	125	-	Ohm
Clock frequency	F_{CLK}	1 LSB current	-	32	-	kHz
Clock input duty cycle	S	-	45	50	55	%
Clock signal period jitter	T_{JIT}	-	-	-	50	nS
Full-scale ADC voltage	V_{FS}	-	-	2.5	VDD	V
Current consumption	I_{DD*}	-	-	-	0.002	mA
		-	0.05	0.1	0.15	
		Mode = "00"	0.05	0.1	0.15	
		Mode = "01"	0.05	0.1	0.2	
	I_{STB}	Mode = "10"	15	100	500	nA
Input logic high level	V_{IH}	Mode = "11"	V_{DD}-0.25	-	V_{DD}+0.25	V
Input logic low level	V_{IL}		-0.25	-	0.25	V

Note: * - excluding load current and VFS current consumption