2/64/128 CMOS/ECL PLL high-frequency divider

SPECIFICATION

1 FEATURES

- TSMC BiCMOS 0.18 um
- Fixed dividing ratio 128 with complementary outputs of dividers on 2 and 64
- Two divider types: CMOS and ECL
- Temperature dependent mode of reference current
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The CMOS high-frequency divider consists of two independent circuits. The first divider is a set of serially connected CMOS dividers with a dividing ratio 2. The second circuit is based on ECL logic and has differential signal. The reference current source of ECL circuit has temperature dependent and temperature independent modes. The buffer-commutators are used to output the signal of a frequency divided by 2, 64 or 128.
The block is fabricated on TSMC BiCMOS 0.18 um technology.

4 STRUCTURE

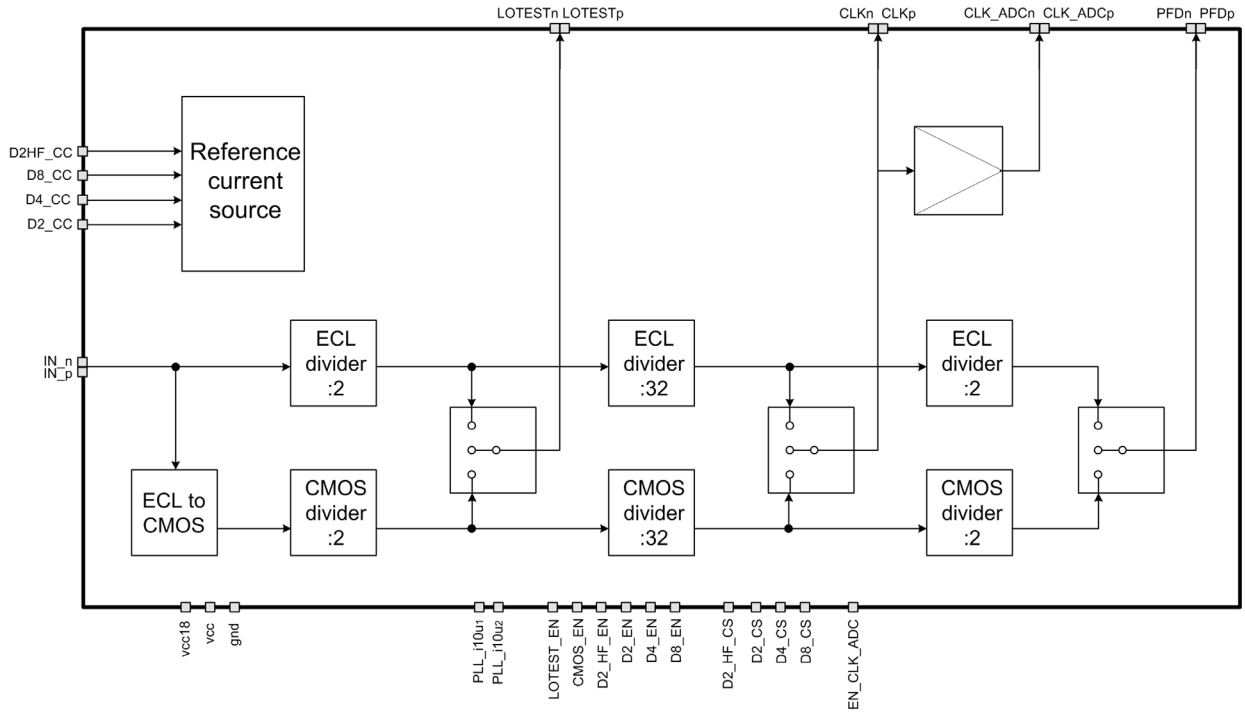

Figure 1: 2/64/128 CMOS/ECL PLL high-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
PLL_i10u$_1$	I	Reference current 10 uA
PLL_i10u$_2$	I	Reference current 10 uA
DIV2_PLL_EN	I	Enable/disable of an input divider by 2
DIV2_EN	I	Enable/disable of an output divider by 2
DIV4_EN	I	Enable/disable of an output divider by 4
DIV8_EN	I	Enable/disable of an output divider by 8
CMOS_EN	I	Divider operating mode selection (CMOS/ECL)
LOTEST_EN	I	Enable/disable of an output buffer for divided by 2 signal
INp	I	Analog differential input
INn	I	
D2_PLL_CC	I	Current consumption control of a PLL divider by 2
D2_CC	I	Current consumption control of a divider by 2
D4_CC	I	Current consumption control of a divider by 4
D8_CC	I	Current consumption control of a divider by 8
D2_PLL_TD	I	Digital code defined the ECL PLL divider by 2 current source type (temperature independent/temperature dependent)
D2_TD	I	Digital code defined the ECL divider by 2 current source type (temperature independent/temperature dependent)
D4_TD	I	Digital code defined the ECL divider by 4 current source type (temperature independent/temperature dependent)
D8_TD	I	Digital code defined the ECL divider by 8 current source type (temperature independent/temperature dependent)
EN_CLK_ADC	I	Enable/disable of an output buffer for divided by 64 signal
LOTESTp	O	Output of a divider by 2
LOTESTn	O	
CLKp	O	Output of a divider by 64
CLKn	O	
PFDp	O	Output of a divider by 128
PFDn	O	
CLK_ADCp	O	Buffer output of a signal divided by 64
CLK_ADCn	O	
vcc18	IO	Supply voltage 1.8 V
vcc	IO	Supply voltage 3.3 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The 2/64/128 CMOS/ECL PLL high frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	450	um
Width	200	um

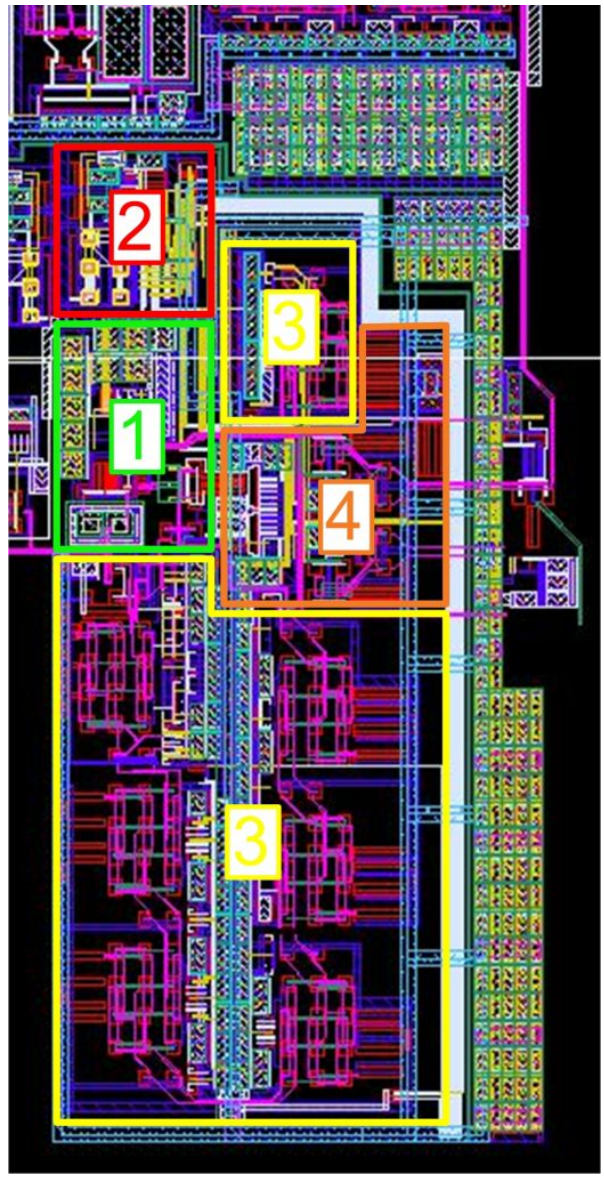

Figure 2: Frequency divider layout

1. CMOS dividers
2. Reference current source
3. ECL dividers
4. Output buffers

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC BiCMOS 0.18 um
Status silicon proven
Area 0.09 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc_18} = 1.7 ÷ 2.2 V, V_{cc} = 2.8 ÷ 4.5 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc_18} = 1.8 V, V_{cc} = 3.3 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition		Value			Unit
				min	typ.	max	
Supply voltage	V_{cc_18}	-		1.7	1.8	2.2	V
	V_{cc}	-		2.8	3.3	4.5	
Operating temperature range	T_j	-		-40	+27	+85	°C
Dividing ratio	R	-		-	128	-	-
Input frequency	F_{IN}	-		500	3200	4500	MHz
Peak-to-peak input voltage	A_{in_in}	-		0.4	0.6	-	V
Peak-to-peak output voltage	A_{out_p-p}	For outputs PFDp и PFDn, CLKp and CLKn		-	0.3	-	V
		For outputs LOTESTp and LOTESTn, CLK_ADCp and CLK_ADCn			0.5		
Supply current	I_{cc}	CMOS mode	F_{IN}= 500 MHz	-	0.84	-	mA
			F_{IN} = 2500 MHz		1.05		
			F_{IN} = 4500 MHz		1.25		
		ECL mode	F_{IN} = 500 MHz		2.36		
			F_{IN} = 2500 MHz		2.36		
			F_{IN} = 4500 MHz		2.36		
Stand-by current	I_{st}	-		-	5	-	nA
Input logic-level high	V_{IH}	For digital inputs		0.9V_{cc}	-	1.1V_{cc}	V
Input logic-level low	V_{IL}			-0.2	-	0.2	V

8 DELIVERABLES

IP block package includes:

- Schematic or NetList
- Abstract model (.lef and .lib files)
- Layout view (optional)
- Behavioral model (Verilog)
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation