Programmable 9-bit CMOS low-frequency divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Range of division ratio from 5 to 511
- Compact structure
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The programmable CMOS low-frequency divider design is based on the 9-bit counter. Since this structure consists of the static triggers, current consumption is closed to zero when there is no input clock. The division ratio is defined by the digital code R<8:0>.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

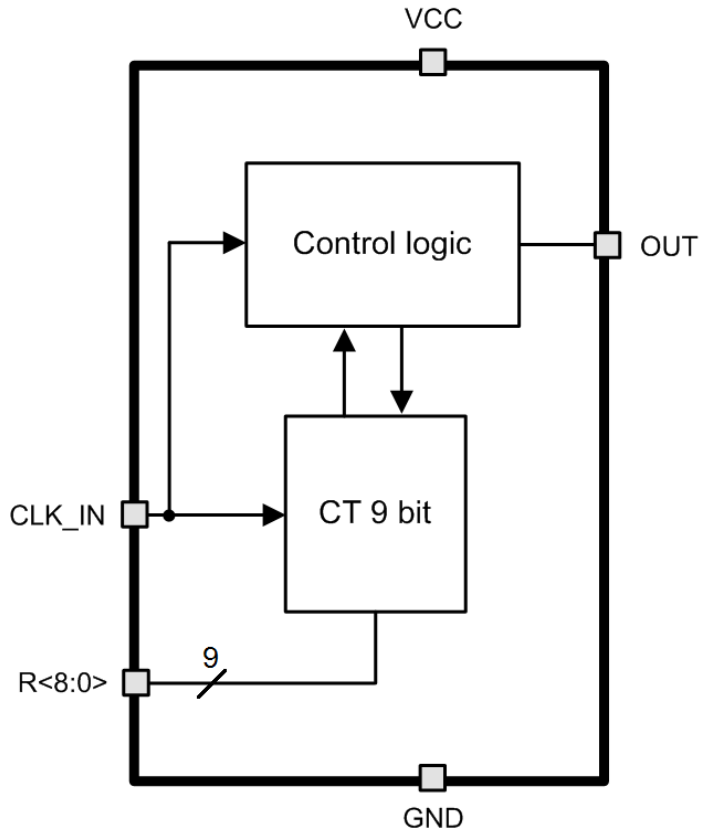

Figure 1: Programmable 9-bit CMOS low-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
CLK_IN	I	Digital input
R<8:0>	I	Digital code of division ratio
OUT	O	Digital output
VCC	IO	Supply voltage 2.0 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable 9-bit CMOS low-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	32	um
Width	88	um

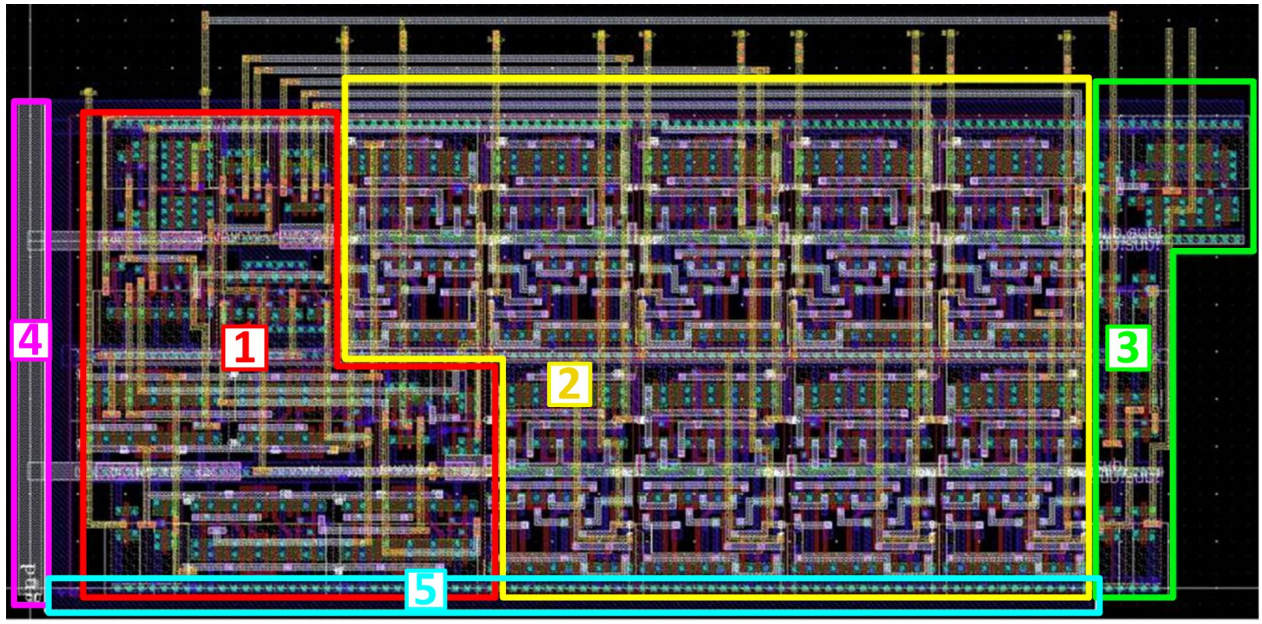

Figure 2: Programmable 9-bit CMOS low-frequency divider layout

1. Control logic
2. Asynchronous counter 9-bit
3. Buffer
4. Ground bus
5. Supply voltage bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 0.003 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.8 ÷ 2.2 V and T_j = -40 ÷ + 85 °C. Typical values are at V_{cc} = 2.0 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.8	2	2.2	V
Operating temperature range	T_j	-	-40	27	+85	°C
Division ratio	R	-	5	-	511	-
Input frequency	F_{IN}	-	-	26	300	MHz
Peak-to-peak input voltage	A_{in_in}	-	1.8	2	2.2	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	1.8	2	2.2	V
Supply current	I_{cc}	F_{IN} = 26 MHz	-	12.3	14.5	uA
		F_{IN} = 50 MHz	-	23.8	28	
Stand-by current	I_{st}	-	-	0.8	35.3	nA
Input logic-level high	V_{IH}	For digital input	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

IP block package includes:

- Schematic or NetList
- Abstract model (.lef and .lib files)
- Layout view (optional)
- Behavioral model (Verilog)
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation