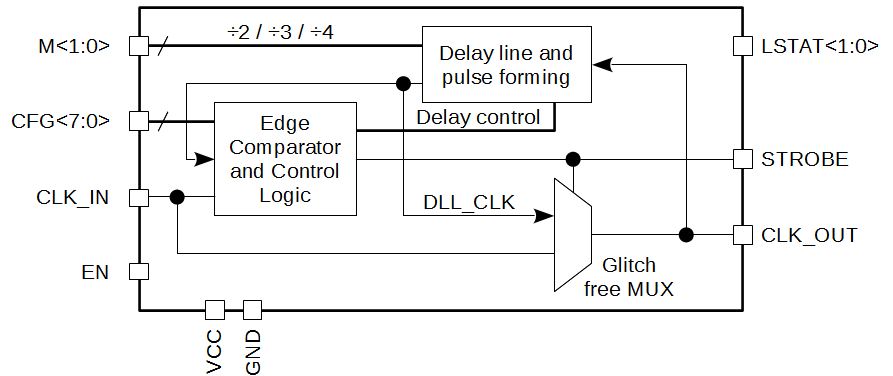


## 10 – 200 MHz DLL-based frequency multiplier

### OVERVIEW

DLL-based frequency multiplier is a simple to configure and operate block, combining, small area and low current consumption. Block wakes up in “pass-through” mode with redirecting input reference frequency to the output. After being configured and enabled the block waits until DLL locks and then switches output clock signal CLK\_OUT to higher frequency.



Disabling block switches it back to “pass-through” mode. Any mode switching is glitch-protected.

IP technology: GlobalFoundries 55 nm.

IP status: silicon proven.

Layout dimensions: 0.440x0.209mm. Total area: 0.092 mm<sup>2</sup>.

### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit	
			min	typ.	max		
Supply voltage	V <sub>CC</sub>	Core voltage	1.1	1.2	1.3	V	
Die temperature	T <sub>j</sub>	-	-40	27	125	°C	
Block current consumption	I <sub>STARTUP</sub>	During 1µs after signal EN goes from signal pass-through to DLL clock output	-	-	4	mA	
	I <sub>ACTIVE</sub>	Active mode F <sub>CLK_OUT</sub> =200MHz	-	230	490		
	I <sub>PASS</sub>	Pass through mode, signal pass-through	F <sub>REF_IN</sub> =10MHz	-	5	20	µA
			F <sub>REF_IN</sub> =50MHz	-	25	40	
			F <sub>REF_IN</sub> =100MHz	-	40	70	
		Pass through mode, DLL clock output, M = 1	F <sub>REF_IN</sub> =10MHz	-	140	250	
F <sub>REF_IN</sub> =50MHz	-		220	400			
F <sub>REF_IN</sub> =100MHz	-		290	490			
Reference frequency range	F <sub>CLK_IN</sub>	-	0.01	-	100	MHz	
CLK_OUT max frequency	F <sub>OUTMAX</sub>	-	200	-	-	MHz	
CLK_OUT min frequency	F <sub>OUTMIN</sub>	Note1	11.5	18	26	MHz	
		Note2	5	8	13		
		Note3	9	16	23		
		Note4	2.5	4	7.5		
CLK_IN duty cycle	CKI <sub>DC</sub>	-	40	50	60	%	
CLK_OUT duty cycle	CKO <sub>DC</sub>	DLL is locked	40	50	60	%	
Delay between rising edge of CLK_IN and following rising edge of CLK_OUT	T <sub>LATIO</sub>	-	-	0.270	0.5	ns	
CLK_IN period jitter <sup>1)</sup>	T <sub>J IN</sub>	-	-	200	-	ps	
CLK_OUT period jitter <sup>1)</sup> with power supply noise	T <sub>JPSN</sub>	M=4	F <sub>CLK_OUT</sub> =4MHz	-	8	-	ns
			F <sub>CLK_OUT</sub> =12MHz	-	3	-	
			F <sub>CLK_OUT</sub> =24MHz	-	1.6	-	
			F <sub>CLK_OUT</sub> =48MHz	-	0.7	-	
			F <sub>CLK_OUT</sub> =100MHz	-	0.4	-	
			F <sub>CLK_OUT</sub> =200MHz	-	0.3	-	
Input logic-high level	V <sub>IH</sub>	For digital inputs	0.8*V <sub>CC</sub>	-	V <sub>CC</sub> +0.1	V	
Input logic-low level	V <sub>IL</sub>		-0.1	-	0.2*V <sub>CC</sub>	V	

Note: 1) Absolute value of period deviation from period nominal (expected) value