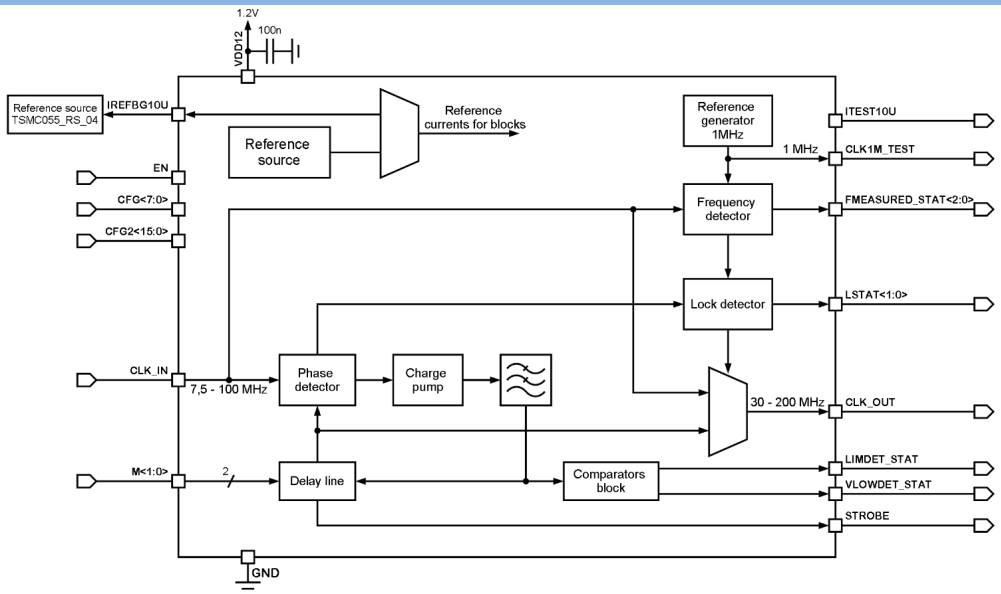
30 – 200 MHz DLL-based frequency multiplier

OVERVIEW



055TSMC_DLL_01 is a frequency multiplier that combines low phase jitter of clock signal, small area and low current consumption. Block wakes up in "pass-through" mode and passes the input signal to the output. Once configured and enabled the block waits until DLL locks and then switches output clock signal CLK_OUT to higher frequency. Disabling block switches it back into "pass-through" mode. Any mode switching is glitch-protected.

IP technology: TSMC 55 nm EF technology.

IP status: pre-silicon verification.

Area: 0.27×0.21 mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				Min	Typ.	Max	
Supply voltage	VDD12	-		1.08	1.2	1.32	V
Operating temperature range	Tj	-		-40	27	+85	°C
Block current consumption	$I_{STARTUP}$	During 1 us after signal EN goes from signal pass-through to DLL clock output		-	-	3	mA
	I_{ACTIVE}	Active mode F_{CLK_OUT} = 200 MHz		-	0.3	1	mA
	I_{PASS}	Pass through mode, EN = "0"	F_{CLK_IN} = 10 MHz	-	10	20	uA
			F_{CLK_IN} = 50 MHz	-	25	40	
			F_{CLK_IN} = 100 MHz	-	45	60	
		Pass through mode, EN = "1", M = "00"	F_{CLK_IN} = 10 MHz	-	115	140	
			F_{CLK_IN} = 50 MHz	-	190	220	
			F_{CLK_IN} = 100 MHz	-	300	320	
Input frequency	F_{CLK_IN}	-		7.5	-	100	MHz
Output frequency	F_{OUTMAX}	-		30	-	200	MHz
CLK_IN duty cycle	CKI_{DC}	-		40	50	60	%
CLK_OUT duty cycle	CKO_{DC}	DLL is locked		40	50	60	%
Delay between rising edge of CLK_IN and following rising edge of CLK_OUT	T_{LATIO}	-		-	0.4	1	ns
CLK_IN period jitter[1)]	T_{J_IN}	-		-	100	-	ps
CLK_OUT period jitter[1)] with power supply noise	T_{JPSN}	F_{OUT} = 200 MHz		-	0.10	0.2	ns
		F_{OUT} = 80 MHz		-	0.15	0.3	
		F_{OUT} = 40 MHz		-	0.3	0.7	
		F_{OUT} = F_{OUTMIN}, LSTAT<1:0> = "10"		-	1.5	3	
		F_{OUT} = F_{OUTMIN}, LSTAT<1:0> = "11"		-	2.1	5	
Input logic-high level	V_{IH}	For digital inputs		0.8*VDD12	-	VDD12	V
Input logic-low level	V_{IL}			0	-	0.2*VDD12	V
Output logic-high level	V_{OH}	For digital outputs		0.8*VDD12	-	VDD12	V
Output logic-low level	V_{OL}			0	-	0.2*VDD12	V

Note: 1) Absolute value of period deviation from period nominal (expected) value.