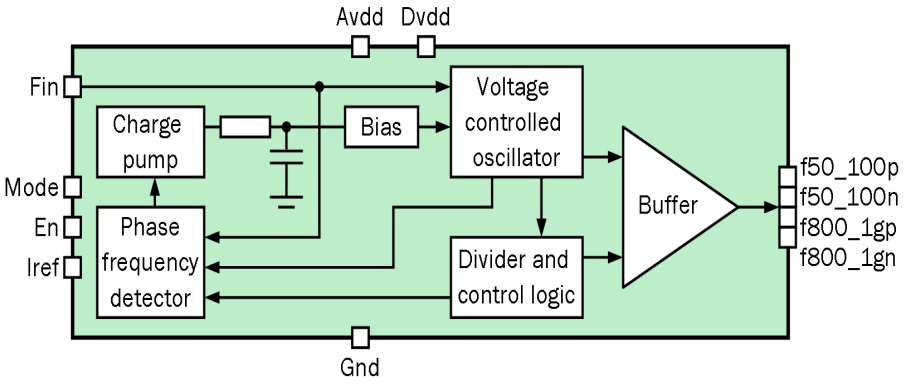
800/1000 MHz DLL-based frequency multiplier

OVERVIEW

090TSMC_MDLL_01 is a clock multiplier accept an input clock and generates a phase-locked output clock at a multiple of the input clock frequency. As with a DLL, each rising edge of the input clock zeros the phase error of the loop. Hence this circuit combines the low phase noise of a DLL with the clock multiplication ability of a PLL.



A divide-by-M counter provides a programmable multiplication ratio for the MDLL.
IP technology: TSMC CMOS Logic Process 90nm.
IP status: silicon proven.
Area: 0.0035mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{Avdd}	-	0.95	1	1.05	V
	V_{Dvdd}	-	0.95	1	1.05	
Power consumption	P_{dd}	F_{800_1g} = 1 GHz	0.95	1	1.05	mW
Operating temperature range	T_j	-	-40	27	125	°C
Input frequency	F_{in}	-	-	50	-	MHz
Multiplying ratio	N	-	-	16/20	-	-
Output frequency	F_{800_1g}	Mode = “0”	-	800	-	MHz
		Mode = “1”	-	1000	-	
Output duty cycle	S	-	-	51	-	%
Jitter (root mean square)	J_{rms}	F_{800_1g} = 1 GHz	5.5	6	6.5	ps
Lock time	T_{lock}	-	2	5	10	us
Input logic-level high	V_{IH}	For digital inputs	0.7	-	-	V
Input logic-level low	V_{IL}		-	-	0.3	V