Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Differential inputs, outputs
- High frequency 0.035 – 170 MHz
- High linearity
- Automatic gain control (AGC) system
- AGC detector threshold adjustment in the digital mode
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- IF signal processing

3 OVERVIEW

IFA consists of 6-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output.
Gain is sequentially reduced from the last stage to the first stage. This method allows to keep a low noise figure in wide gain range.
The IFA is designed using TSMC CMOS 65 nm technology.

4 STRUCTURE

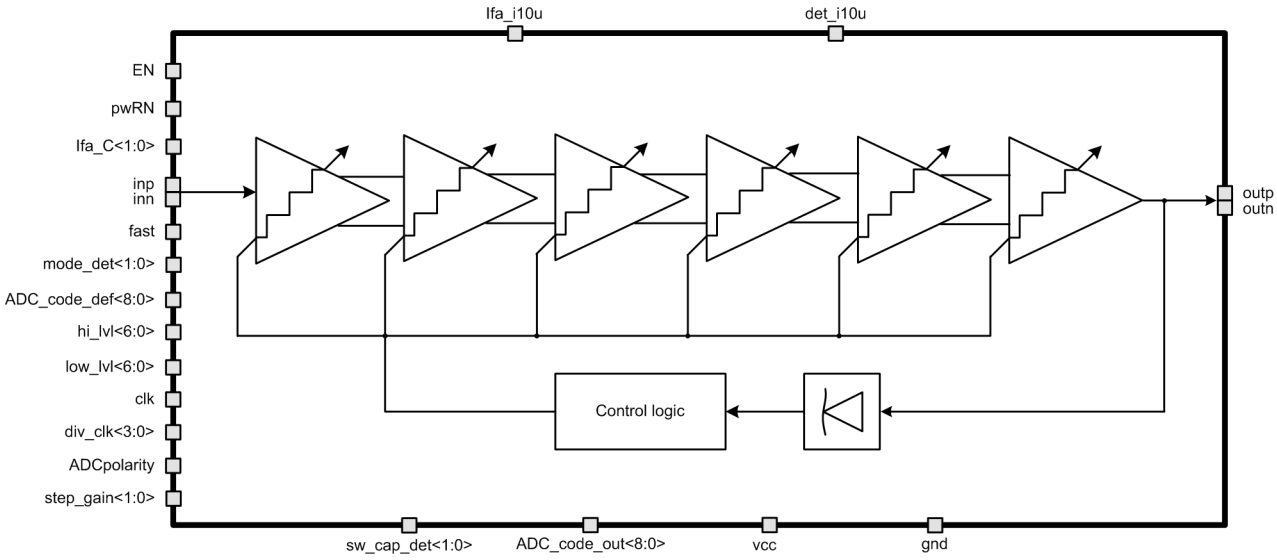

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
ifa_i10u	I	IFA reference current 10 uA
det_i10u	I	Detector reference current 10 uA
inp	I	IFA differential input
inn	I	
EN	I	IFA enable/disable
pwRN	I	Reset to default
ifa_CC<1:0>	I	IFA current consumption control
fast	I	IFA enable bit fast amplitude adjustment
mode_det<1:0>	I	Detector mode
ADC_code_def<8:0>	I	IFA initial value gain
hi_lvl<6:0>	I	Amplitude detector upper limit
low_lvl<6:0>	I	Amplitude detector lower limit
clk	I	Digital amplitude detector clock input
div_clk<3:0>	I	Digital amplitude detector clock frequency divider
ADCpolarity	I	AGC polarity
step_gain<1:0>	I	Gain adjustment step
sw_cap_det<1:0>	I	Detector capacitor value
ADC_code_out<8:0>	O	IFA gain control
outp	O	IFA differential output
outn	O	
vcc	IO	Supply voltage 2.5 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Low noise amplifier dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	1620	um
Width	600	um

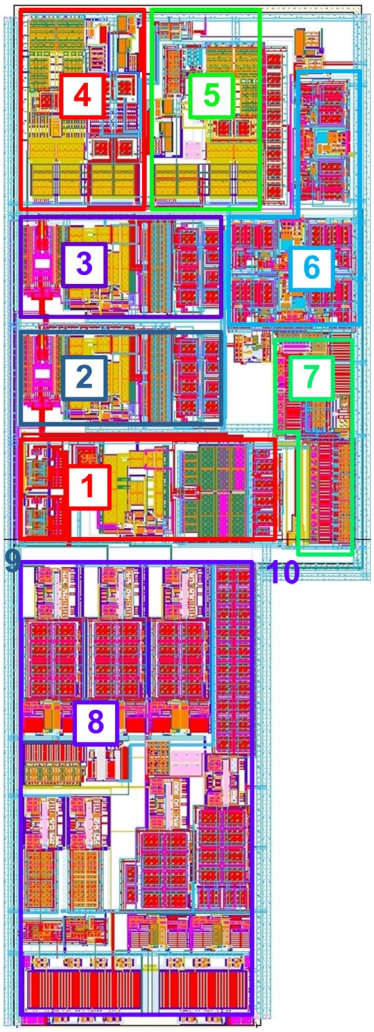

Figure 2: Intermediate-frequency amplifier layout

1. IFA 1st stage
2. IFA 2nd stage
3. IFA 3rd stage
4. IFA linear buffer
5. IFA test buffer
6. DC offset compensation
7. IFA current source
8. Detector
9. Supply voltage
10. Ground

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status pre-silicon verification
Area 0.95 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.375 ÷ 2.625 V and T_j = -40 ÷ +125 °C. Typical values are at V_{cc} = 2.5 V, T_j = +85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.375	2.5	2.625	V
Temperature range	T_j	-	-40	85	+125	°C
Supply current	I_{cc}	-	-	215	-	mA
Stand-by current	I_{stb}	-	-	5	-	uA
Band pass	F	-	0.035	-	170	MHz
Maximum gain	Gmax	-	67	71	83	dB
Minimum gain	Gmin	-	-0.4	0.5	3.6	dB
Gain control step	k	Step preset	0.1	-	0.5	dB
Amplitude ripple	R_{PAF}	-	-	1.1	2	dB
Group delay ripple	RP_{gvz}	IF band 1 MHz - 100 MHz	-	32	43	ns
Input 1dB compression point	P_{1dB}	Gmin	9.5	11	-	dBm
Third order intermodulation	IM3	1 V(p-p)	-43	-58	-	dB
Noise figure	NF	Minimum gain	-	31	32	dB
		Gain > 15 dB	-	18.7	19.1	dB
		Gain > 30 dB	-	13.5	14	dB
Common mode	V_{IFA_dif}	Output	-	0.6	-	V
Input impedance	R	Differential input	-	50	-	Ohm
Input logic-level high	V_{IH}	For digital input	$0.85V_{cc}$	-	$1.15V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 TYPICAL CHARACTERISTICS

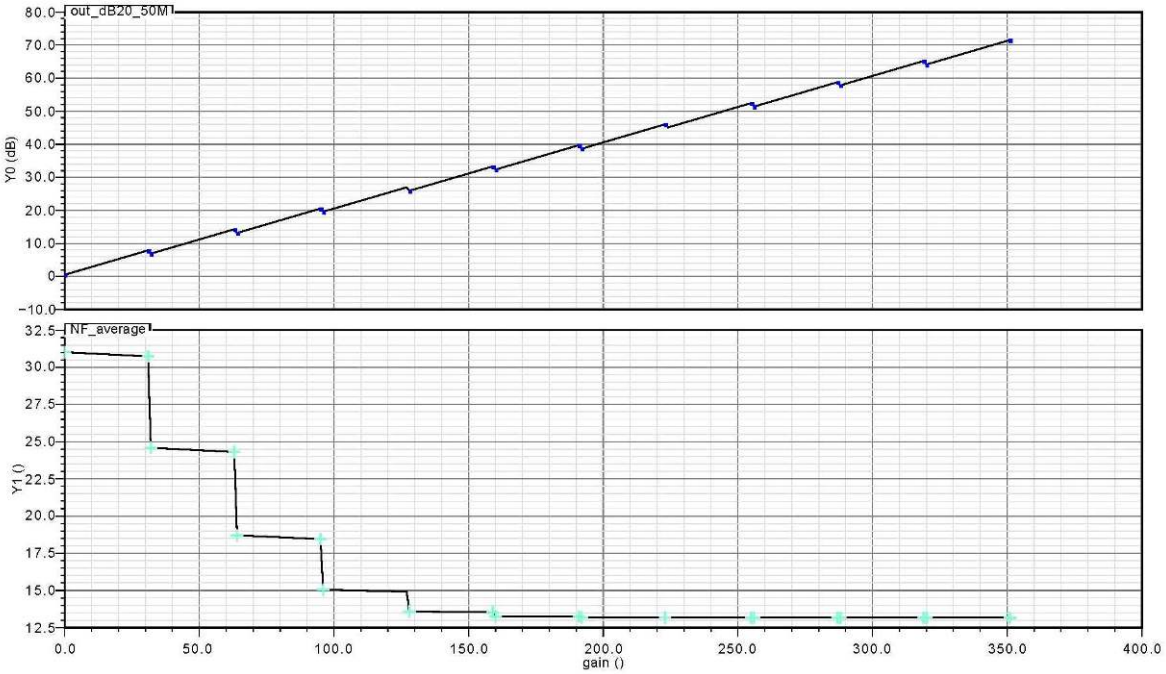

Figure 3: Gain characteristics, NF over code IFA

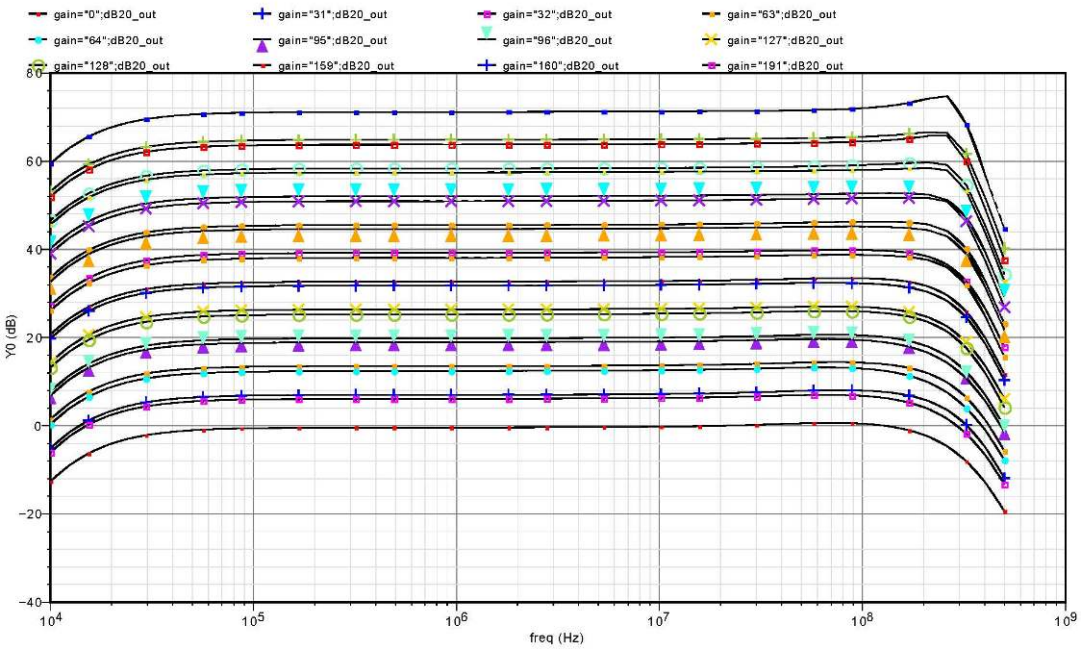

Figure 4: Amplitude frequency characteristics over gain code IFA

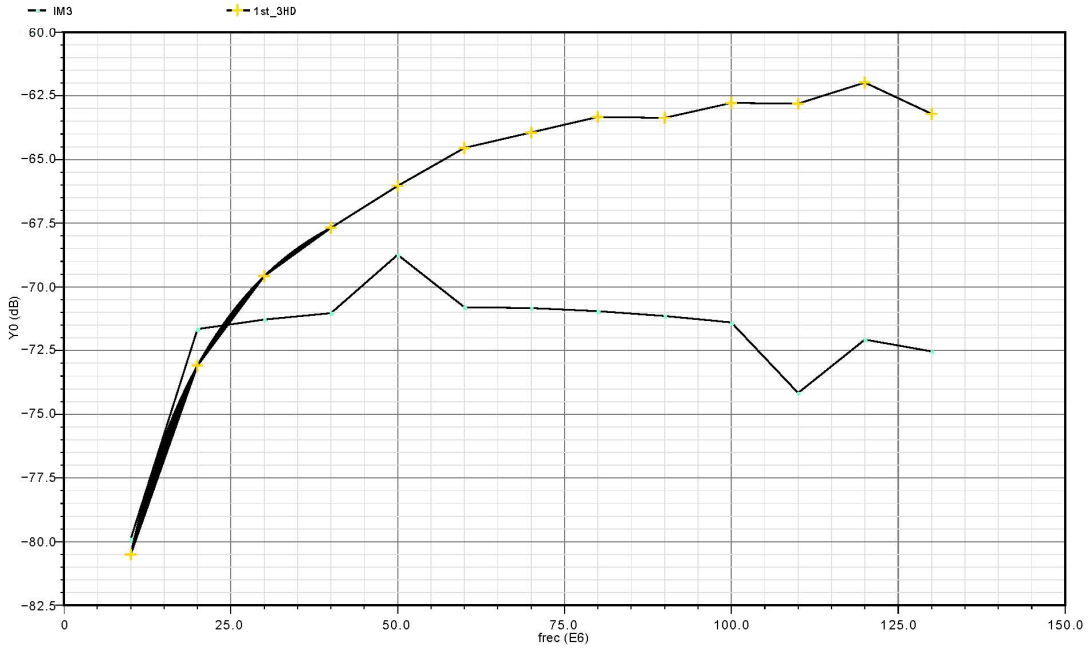

Figure 5: IM3 and HD3 (min gain, Vout=1V_{p-p})

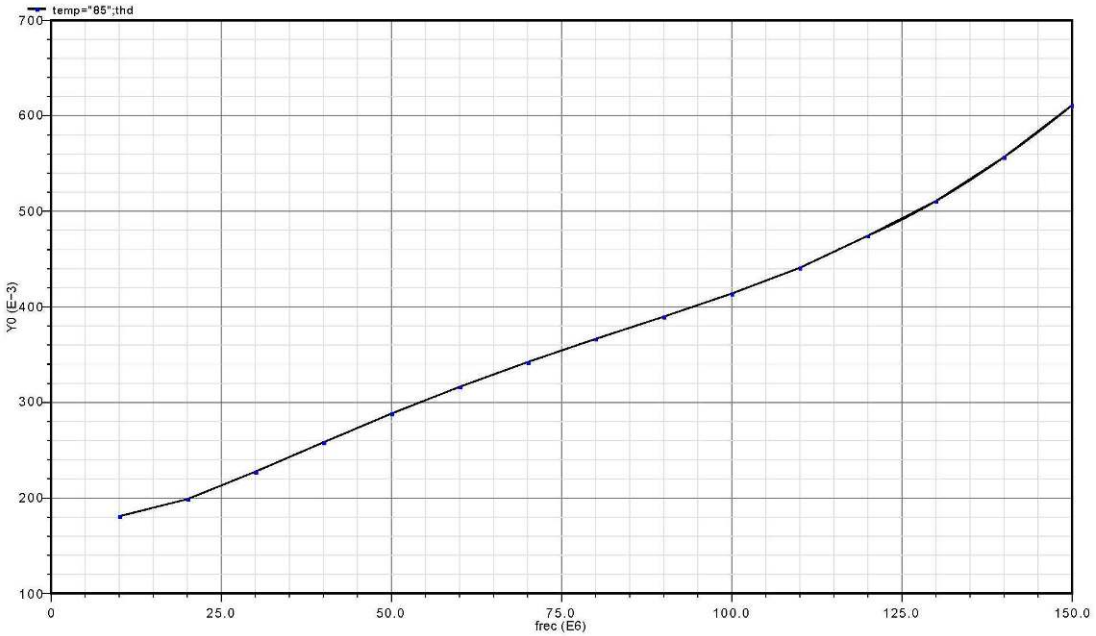

Figure 6: Thd (min gain, Vout=1V_{p-p})

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation