Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18 um
- Wide gain range (0…62 dB)
- Low group delay time ripple vs. frequency and gain
- Analog and digital output modes
- Built-in AGC detector with external capacitor
- On-board bias compensation on dc voltage in each amplifier stage and output buffer
- Usage of ADC for the purpose of receipt of digital output signal
- Portable to other technologies (upon request)

2 APPLICATION

- Receivers
- Transceivers
- Navigation systems

3 OVERVIEW

IFA consists of 3-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for 2-bits digital output.
Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the last stage to the first stage. Also gain can be fixed by the digital code DAC<9:0>.
Output voltage supported by AGC system on differential load at 500 Ohm or 1000 Ohm compounds:

- For sine waveform 200 mV (peak-to-peak)
- For noise signal 480 mV (peak-to-peak)

The block is fabricated on SMIC CMOS 0.18 um technology.

4 STRUCTURE

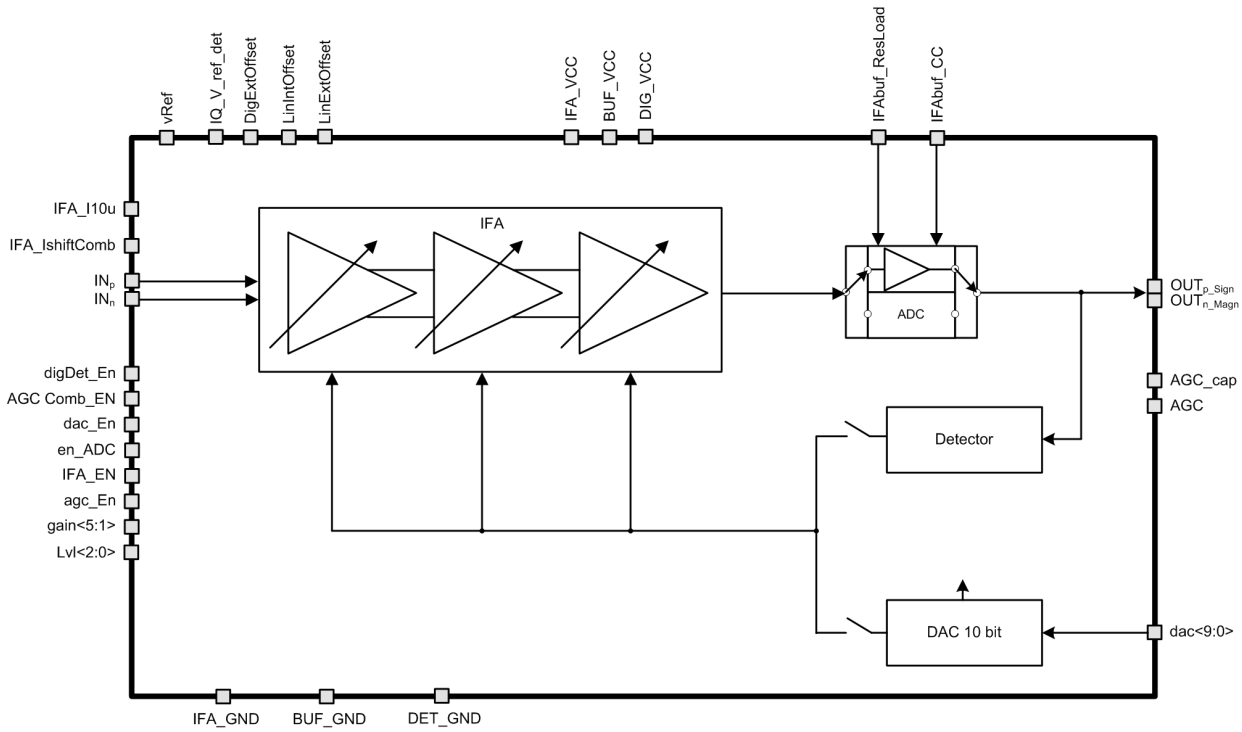

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
IFA_I10u	I	Reference current 10 uA
IFAbuf_CC	I	Linear buffer current consumption control
IQ_V_ref_det	IO	AGC voltage output double - channel application
IFA_EN	I	IFA enable/disable
AGC_Comb_EN	I	Switching AGC for double-channel usage
vRef	I	Reference voltage (~ 1.25 V)
INp	I	IFA differential input
INn	I	
DigExtOffset	I	DC offset compensation mode: IFA buffer/ADC output-referred or IFA buffer/ADC input-referred
LinIntOffset	I	
LinExtOffset	I	
gain<5:1>	I	AGC joint adjustment when using double-channel
Lvl<2:0>	I	ADC analog detector threshold setting
IFAbuf_ResLoad	I	Linear buffer load selection (500 Ohm or 1000 Ohm)
digDet_En		ADC detector type (analog/digital)
en_ADC	I	IFA output type (differential linear/digital CMOS)
dac_En	I	IFA AGC mode
agc_En	I	
dac<9:0>	I	DAC digital code (10 bits), setting IFA gain coefficients
AGC	O	External capacitor for AGC
OUT_{p_Sign}	O	IFA differential/digital output
OUT_{n_Magn}	O	
IFA_IshiftComb	O	Reference current output 10 uA
AGC_cap	O	AGC voltage output
IFA_VCC	IO	IFA supply voltage 3.15 V
BUF_VCC	IO	Output buffer supply voltage
DIG_VCC	IO	ADC supply voltage
IFA_GND	IO	IFA ground
BUF_GND	IO	Output buffer ground
DET_GND	IO	Amplitude detector ground

6 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	1020	um
Width	1000	um

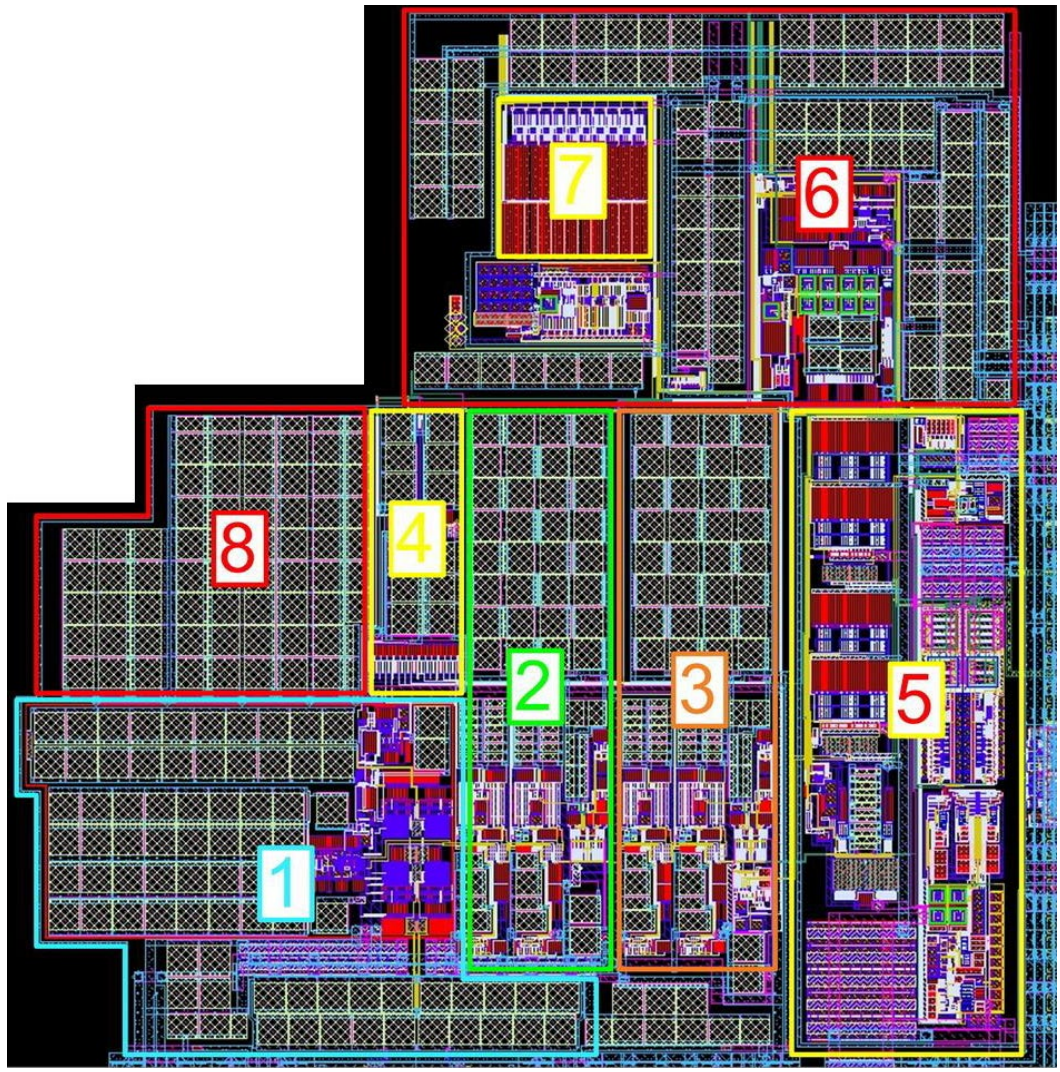

Figure 2: Intermediate-frequency amplifier layout

1. IFA 1st stage
2. IFA 2nd stage
3. IFA 3rd stage
4. IFA reference current source
5. Linear and digital buffer with ADC
6. Linear and digital detector
7. 10 bit DAC
8. Filter capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology SMIC CMOS 0.18 um
Status silicon proven
Area 0.88 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc_IFA} = 3.0 ÷ 3.3 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc_IFA} = 3.15 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc_IFA}	-	3.0	3.15	3.3	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Frequency range	F	-	5	-	20	MHz
Maximal gain	G_{max}	-	62	70	76	dB
Noise figure	NF	-	-	5.7*	7.6*	dB
Group delay time ripple	RP_{AF}	-	-	2.9	3.8	ns
Differential output resistance	R_{IN}	-	1550	1960	2500	Ohm
Peak-to-peak voltage at the differential output	A_{p-p}	-	180	200	226	mV
Output logic-level low (digital outputs)	V_{OH_dig}	For outputs $OUT_{p/Sign}$, $OUT_{n/Magn}$, with ADC mode. Load current 2 mA	V_{cc_IFA}-0.5	V_{cc_IFA}-0.2	V_{cc_IFA}	V
Output logic-level high (digital outputs)	V_{OL_dig}	For outputs $OUT_{p/Sign}$, $OUT_{n/Magn}$, with ADC mode. Load current 2 mA	0	0.04	0.2	V
ADC capacity	K	-	-	1.5	-	bit
Supply current	I_{cc}	Linear mode	-	3.4	4	mA
		ADC mode, 10 MHz	-	4.9	6.1	mA
Stand-by current	I_{stb}	-	-	0.01	0.15	uA
Input logic-level high	V_{IH}	For digital inputs	0.7V_{cc_IFA}	-	V_{cc_IFA}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Note:
* - with voltage gain coefficient over 30 dB
** - for sinusoidal signal

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation