# 5 to 20MHz Intermediate frequency amplifier

OVERVIEW

180SMIC_IFA_02 consists of 3-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for 2-bits digital output. Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the last stage to the first stage. Also gain can be fixed by the digital code **DAC<9:0>**. Output voltage supported by AGC system on differential load at 500Ohm or 1kOhm compounds: for sine waveform 200 mV (peak-to-peak); for noise signal 480 mV (peak-to-peak).
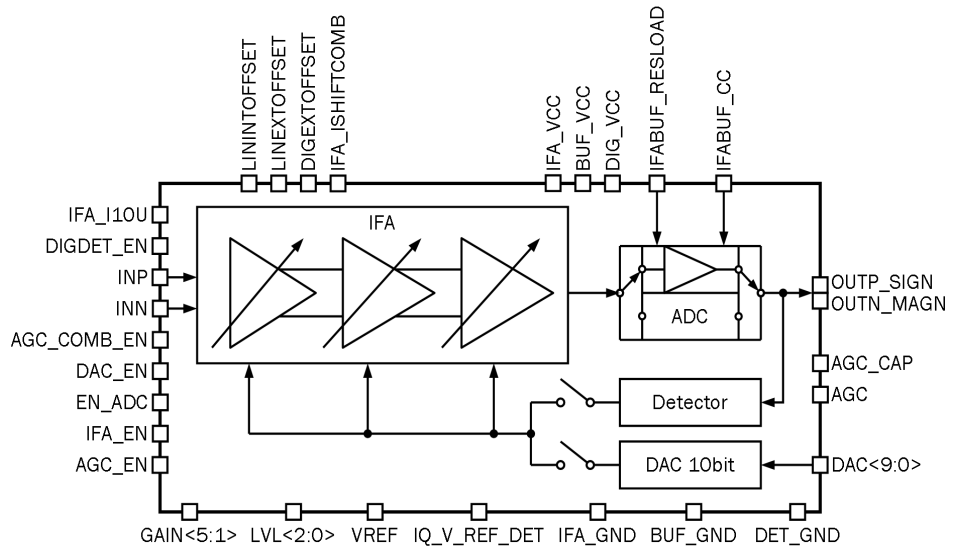
IP technology: SMIC CMOS 180 nm.
IP status: silicon proven.
Area: 0.88mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{CC_IFA}	-	3.0	3.15	3.3	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Frequency range	F	-	5	-	20	MHz
Maximal gain	G_{max}	-	62	70	76	dB
Noise figure	NF	-	-	5.7*	7.6*	dB
Group delay time ripple	RP_{AF}	-	-	2.9	3.8	ns
Differential output resistance	R_{IN}	-	1550	1960	2500	Ohm
Peak-to-peak voltage at the differential output	A_{p-p}	-	180	200	226	mV
Output logic-level low (digital outputs)	V_{OH_dig}	For outputs $OUT_{p/Sign}$, $OUT_{n/Magn}$, with ADC mode. Load current 2 mA	V_{CC_IFA}-0.5	V_{CC_IFA}-0.2	V_{CC_IFA}	V
Output logic-level high (digital outputs)	V_{OL_dig}	For outputs $OUT_{p/Sign}$, $OUT_{n/Magn}$, with ADC mode. Load current 2 mA	0	0.04	0.2	V
ADC capacity	K	-	-	1.5	-	bit
Supply current	I_{cc}	Linear mode	-	3.4	4	mA
		ADC mode, 10 MHz	-	4.9	6.1	mA
Stand-by current	I_{stb}	-	-	0.01	0.15	uA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{CC\_IFA}$	-	V_{CC_IFA}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Note:
* - with voltage gain coefficient over 30 dB