

# Intermediate-frequency amplifier

## SPECIFICATION

### 1 FEATURES

- TSMC SiGe BiCMOS 0.18 um
- Wide gain range (0...62 dB)
- Low group delay time ripple vs. frequency and gain
- Analog and digital output modes
- Automatic gain control (AGC) system
- AGC detector threshold adjustment in the digital mode
- Portable to other technologies (upon request)

### 2 APPLICATION

- Receivers

### 3 OVERVIEW

IFA consists of 3-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for 2-bits digital output.

Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the last stage to the first stage. Also gain can be fixed by the digital code DAC<9:0>.

The block is fabricated on TSMC SiGe BiCMOS 0.18 um technology.

### 4 STRUCTURE

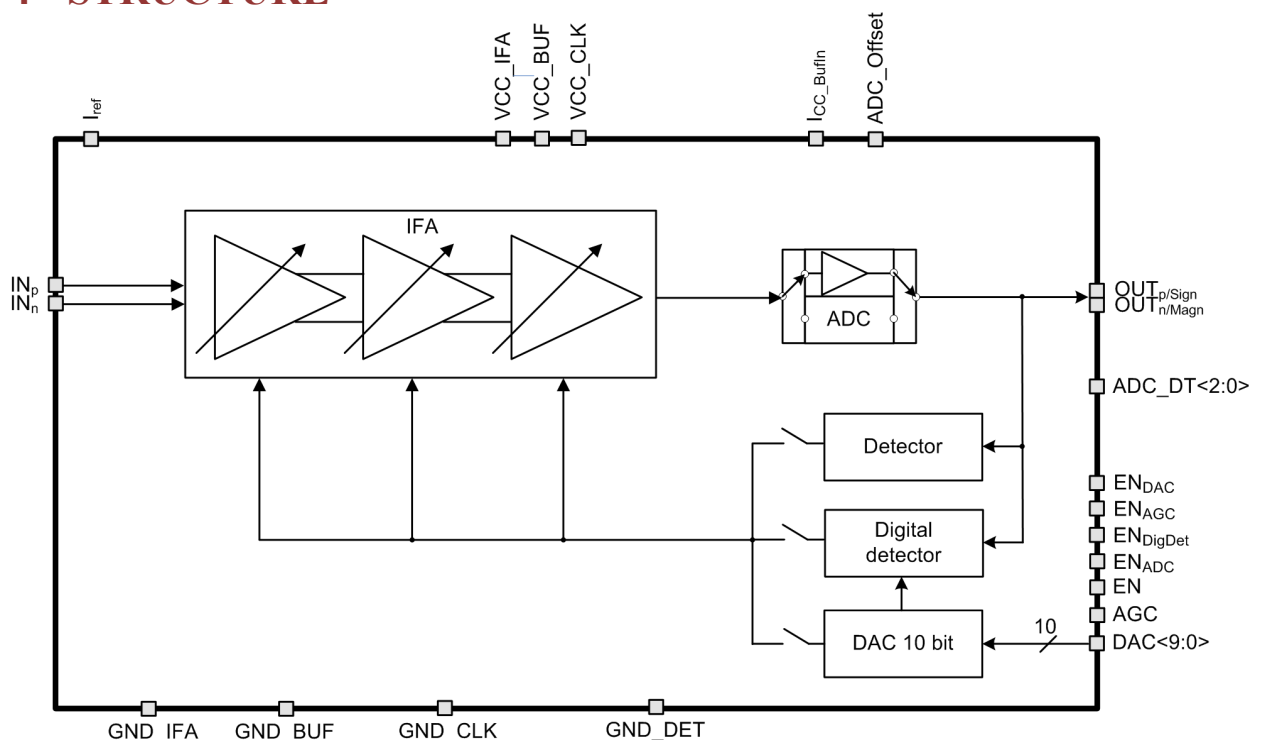


Figure 1: Intermediate-frequency amplifier structure

## 5 PIN DESCRIPTION

Name	Direction	Description
I <sub>ref</sub>	IO	Reference current 10 uA
IN <sub>p</sub>	I	Differential input
IN <sub>n</sub>	I	
I <sub>CC_BuffIn</sub>	I	Linear buffer current consumption control
ADC_Offset	I	DC offset compensation mode: IFA buffer/ADC output-referred or IFA buffer/ADC input-referred
ADC_DT<2:0>	I	Digital code defined ADC analog detector threshold
DAC<9:0>	I	Digital code for DAC
EN <sub>DigDet</sub>	I	ADC detector type (analog/digital)
EN <sub>DAC</sub>	I	IFA AGC mode
EN <sub>AGC</sub>	I	
EN <sub>ADC</sub>	I	IFA output type (differential linear/digital CMOS)
EN	I	IFA enable/disable
AGC	IO	External capacitor for AGC
OUT <sub>p</sub> /Sign	O	Differential/digital output
OUT <sub>n</sub> /Magn	O	
VCC_IFA	IO	IFA supply voltage 3.15 V
VCC_BUF	IO	Output buffer supply voltage
VCC_CLK	IO	Digital buffer supply voltage
GND_IFA	IO	IFA ground
GND_BUF	IO	Output buffer ground
GND_CLK	IO	ADC ground
GND_DET	IO	Amplitude detector ground

## 6 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	670	um
Width	753	um

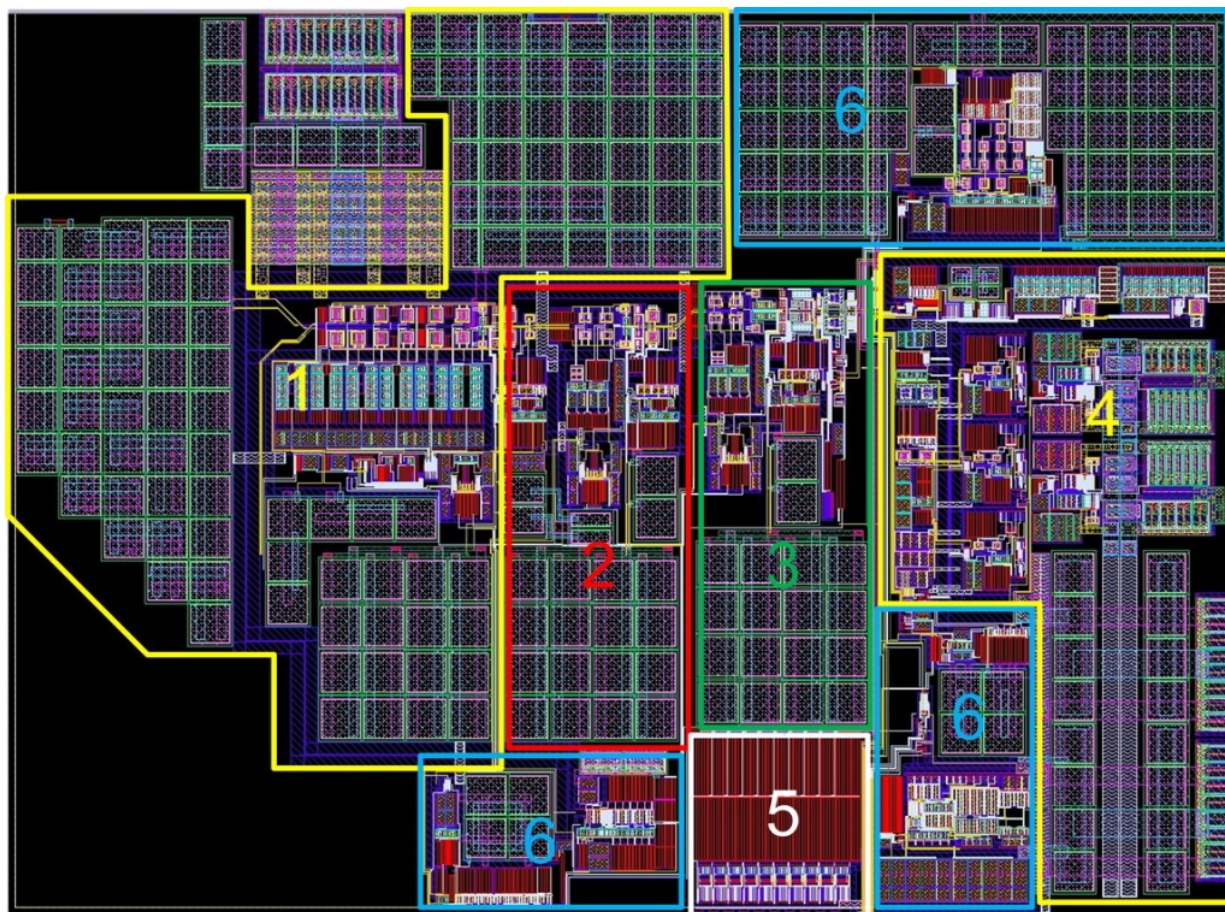


Figure 2: Intermediate-frequency amplifier layout

1. IFA 1<sup>st</sup> stage
2. IFA 2<sup>nd</sup> stage
3. IFA 3<sup>rd</sup> stage
4. Linear and digital buffer with ADC
5. 10 bit DAC
6. AGC system

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC SiGe BiCMOS 0.18 um  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.51 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc\_IFA} = V_{cc\_BUF} = 2.8 \div 3.6$  V and  $T_j = -40 \div +85$  °C. Typical values are at  $V_{cc\_IFA} = V_{cc\_BUF} = 3.15$  V,  $T_j = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{cc\_IFA}$	-	2.8	3.15	3.6	V
	$V_{cc\_BUF}$	-	2.8	3.15	3.6	
Operating temperature range	$T_j$	-	-40	+27	+85	°C
Frequency range	$F_{IN}$	-	5	-	20	MHz
Group delay time ripple	$t_{del}$	-	-	1.6	3.2	ns
Gain	$G_{MAX}$	Maximum	62	70	80	dB
Input resistance	R	-	1.63	2.0	2.3	kOhm
Noise figure	NF	Gain more than 30 dB	-	11.1	12.2	dB
Peak-to-peak voltage at the differential output	$V_{dif\_p-p}$	Differential load 200 Ohm	170	198*	227	mV
DC operating point	$V_{IFA\_dif}$	For outputs $OUT_{p/Sign}$ , $OUT_{n/Magn}$ , linear mode	-	$V_{cc\_BUF}-1.15$	-	V
Output logic-level low (digital outputs)	$V_{OH\_dig}$	For outputs $OUT_{p/Sign}$ , $OUT_{n/Magn}$ , ADC mode. Load current 2 mA	$V_{cc\_BUF}-0.5$	$V_{cc\_BUF}-0.2$	$V_{cc}$	V
Output logic-level high (digital outputs)	$V_{OL\_dig}$	For outputs $OUT_{p/Sign}$ , $OUT_{n/Magn}$ , ADC mode. Load current 2 mA	0	0.04	0.2	V
ADC resolution	$R_{ADC}$	-	-	2	-	bit
Supply current	$I_{cc\_dif}$	Linear mode	-	2.1	2.6	mA
	$I_{cc\_ADC}$	ADC mode, 10 MHz	-	3.8	-	
Stand-by current	$I_{stb}$	-	-	0.01	0.1	uA
Input logic-level high	$V_{IH}$	For digital inputs, ADC_Offset, DAC<9:0>, EN <sub>AGC</sub> , EN <sub>DAC</sub> , EN <sub>DigDet</sub>	$0.7V_{cc\_IFA}$	-	$V_{cc\_IFA}+0.25$	V
		For digital inputs, ADC_DT<2:0>, I <sub>CC_Bufln</sub> , EN, EN <sub>ADC</sub>	$0.7V_{cc\_BUF}$	-	$V_{cc\_BUF}+0.25$	
Input logic-level low	$V_{IL}$	For digital inputs	-0.25	-	0.3	V

Note:

\* – for sinusoidal signal

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation