Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide gain range from 0 to 42 dB
- Wide offset voltage adjustment
- Built-in automatic gain control and DC voltage offset compensation system
- Low input noise
- Small area
- No external components required
- Portable to other technologies (upon request)

2 APPLICATION

- Receivers
- Transceivers

3 OVERVIEW

Intermediate-frequency amplifier consists of 1 stage amplifier with dual (I/Q) differential inputs/outputs, automatic gain control system and output DC voltage offset compensation system based on a digital-to-analog converter.
Output comparators are used to detect the overrunning of nominal output signal values.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

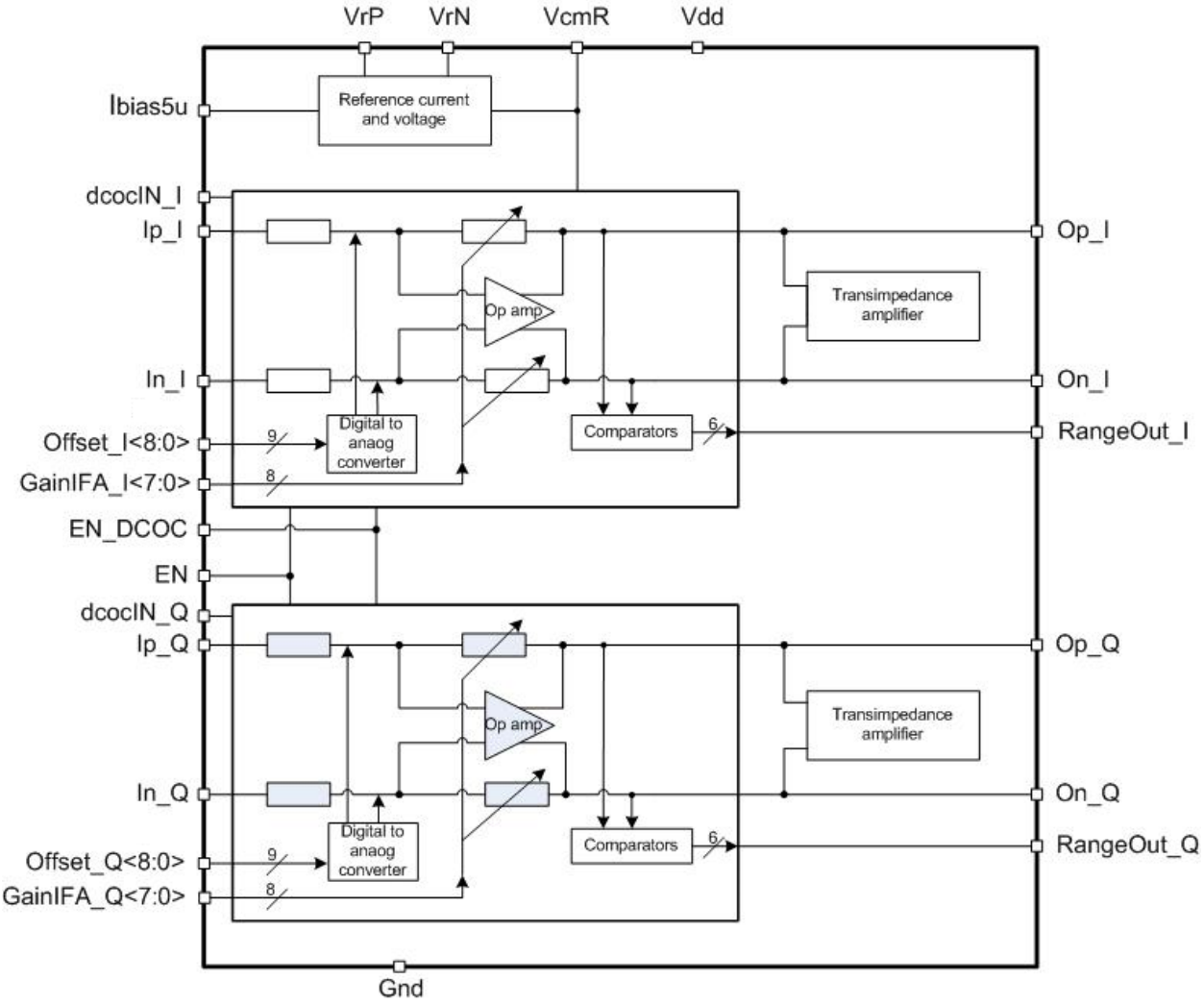

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
Ibias5u	I	Reference current (5 uA)
Ip_I	I	I channel analog differential input
In_I	I	
Ip_Q	I	Q channel analog differential input
In_Q	I	
dcocIN_I	I	External capacitor connection (I channel)
dcocIN_Q	I	External capacitor connection (Q channel)
GainIFA_I<7:0>	I	Gain control (I channel)
Offset_I<8:0>	I	Digital DC voltage offset compensation (I channel)
GainIFA_Q<7:0>	I	Gain control (Q channel)
Offset_Q<8:0>	I	Digital DC voltage offset compensation (Q channel)
EN	I	Enable/disable
EN_DCOC	I	DC voltage offset compensation system enable/disable
Op_I	O	I channel analog differential output
On_I	O	
Op_Q	O	Q channel analog differential output
On_Q	O	
VrP	O	ADC reference voltage (positive reference voltage)
VrN	O	ADC reference voltage (negative reference voltage)
VcmR	O	ADC in-phase component level
RangeOut_I	O	Digital DC offset compensation and gain control (I channel)
RangeOut_Q	O	Digital DC offset compensation and gain control (Q channel)
Vdd	IO	Supply voltage 2.05 V
Gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	500	um
Width	878	um

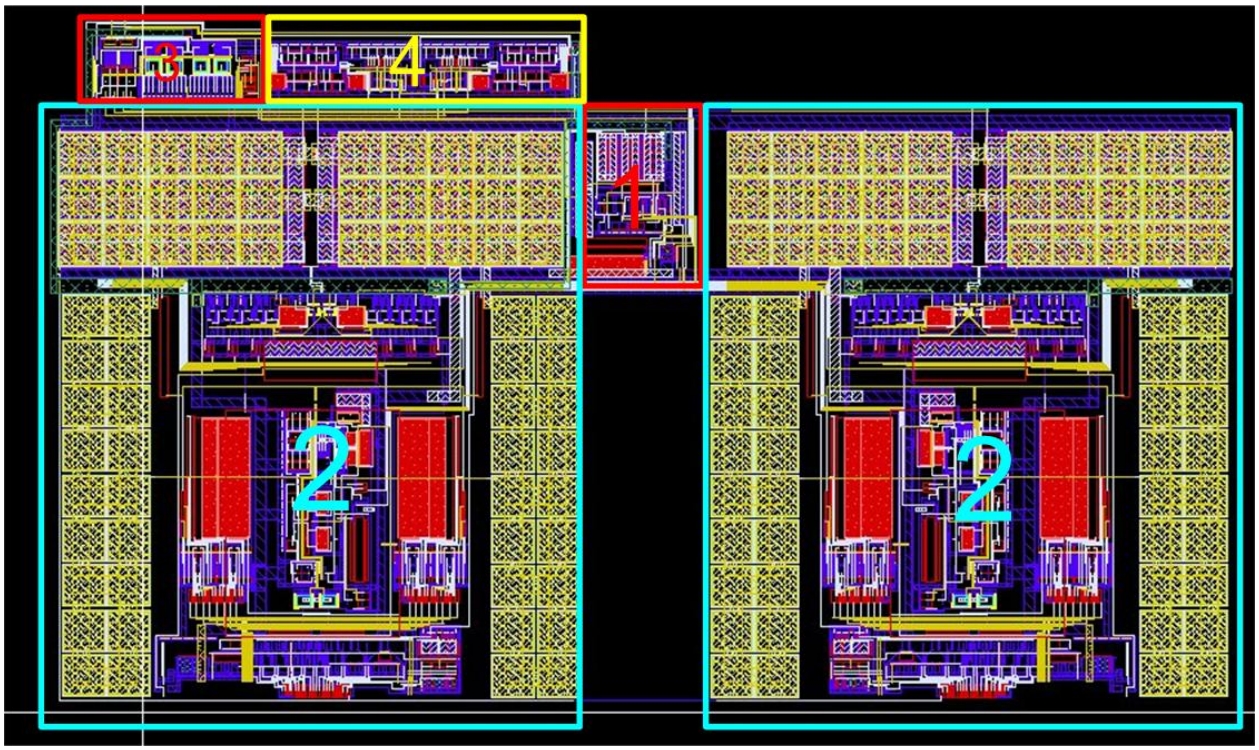

Figure 2: Intermediate-frequency amplifier layout

1. Reference current and voltage system
2. Amplifier with adjusted gain
3. Test buffer
4. Transimpedance amplifier

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 0.4 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.9 ÷ 3.5 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.05 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.9	2.05	3.5	V
Temperature operating range	T_j	-	-45	27	85	°C
Noise figure	NF_{IFA}	Maximum gain	-	6	-	dB
		Minimum gain	-	14	-	dB
Frequency range	F_{IN}	-	0	-	10	kHz
Group delay time ripple	t_{del}	In the bandwidth 10 kHz	-	-	11	us
Gain	G_{IFAmax}	-	0	-	42	dB
Input 1dB compression point	P_{1dB}	Minimum gain	-	-25	-	dBm
		Maximum gain	-	-67	-	
Input impedance	R_{in}	-	-	60	-	kOhm
Output impedance	R_{out}	-	-	20	-	kOhm
Input DC operating point	V_{IFA_in}	-	-	1.43	-	V
Output DC operating point	V_{IFA_out}	-	-	1.1	-	V
Peak-to-peak differential output voltage	$A_{in\ p\text{-}p}$	-	-	560	-	mV
Current consumption in an active mode	I_{cc}	-	-	150	200	uA
Stand-by current	I_{stb}	-	-	2.4	67	nA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Subsection 7.2 update