Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- AMS BiCMOS 0.35 um
- Wide gain range (0…64 dB)
- Low group delay time ripple vs. frequency and gain
- Analog and digital output modes
- Built-in AGC detector with internal capacitor
- Built-in DC offset compensation mode in each stage and in the output buffer
- AGC detector threshold adjustment in the digital mode
- Portable to other technologies (upon request)

2 APPLICATION

- Receivers
- Navigation systems

3 OVERVIEW

IFA consists of 4-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for digital output and a detector of output level.

The amplifier has differential inputs and outputs, and consists of 4 stages. Gain is sequentially reduced from the last stage to the first stage. This method allows to keep a low noise figure in wide gain range.

The output voltage maintained by AGC system at differential load 200 Ohm:

- for sinusoidal signal is 200 mV (p-p);
- for noise signal is 480 mV (p-p).

The block is fabricated on AMS BiCMOS 0.35 um technology.

4 STRUCTURE

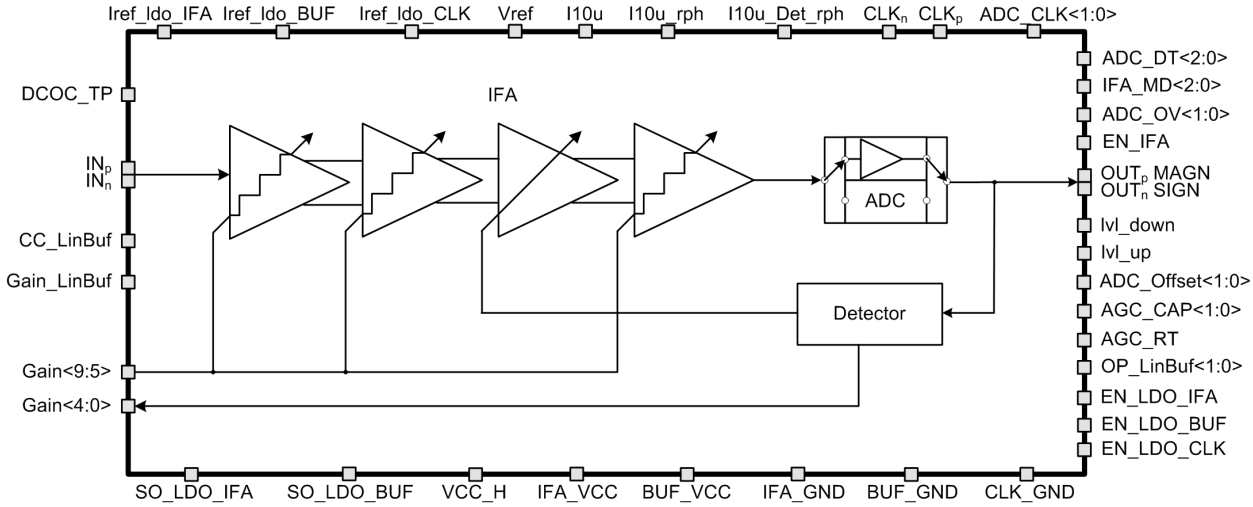

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Descrirtion
EN_LDO_IFA	I	IFA LDO VR enable/disable
EN_LDO_BUF	I	IFA linear buffer LDO VR enable/disable
EN_LDO_CLK	I	IFA digital buffer LDO VR enable/disable
SO_LDO_IFA	I	External power supply enable/disable
SO_LDO_BUF	I	
EN_IFA	I	IFA enable/disable
ADC_OV<1:0>	I	Digital output level
IFA_MD<2:0>	I	IFA mode
Gain<9:5>	I	IFA gain
Gain<4:0>	I	Digital code for DAC
ADC_DT<2:0>	I	Comparator comparison mode (digital mode)
ADC_CLK<1:0>	I	Digital buffer clock mode
OP_LinBuf<1:0>	I	DC linear output level control
AGC_RT	I	AGC capacitor charge current adjustment
AGC_CAP<1:0>	I	AGC capacity control
ADC_Offset<1:0>	I	Digital DC offset compensation mode
lvl_up	O	Detector digital output for IFA gain control
lvl_down	O	
Iref_ldo_IFA	I	Reference current 5 uA
Iref_ldo_BUF	I	Reference current 5 uA
Iref_ldo_CLK	I	Reference current 5 uA
I10u	I	Reference current 10 uA
I10u_rph	I	Reference current with temperature dependence on resistor rphrpoly (10 uA)
I10u_Det_rph	I	Detector reference current with temperature dependence on resistor rphrpoly (10 uA)
Vref	I	Reference supply voltage (~1.133 V)
IN_p	I	Differential input
IN_n	I	
CLK_p	I	Differential clock input
CLK_n	I	
CC_LinBuf	I	Linear buffer current control

Table «Pin description» (continue)

Name	Direction	Descrirtion
Gain_LinBuf	I	Linear buffer gain control
DCOC_TP	I	DC offset compensation mode of IFA buffer/DAC output or input referred
OUTp_MAGN	O	IFA output
OUTn_SIGN	O	
VCC_H	IO	High supply voltage 3.0 V
IFA_VCC	IO	IFA supply voltage 2.7 V
BUF_VCC	IO	IFA buffer supply voltage 2.7 V
IFA_GND	IO	IFA ground
BUF_GND	IO	IFA buffer ground
CLK_GND	IO	IFA digital buffer ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	600	um
Width	2020	um

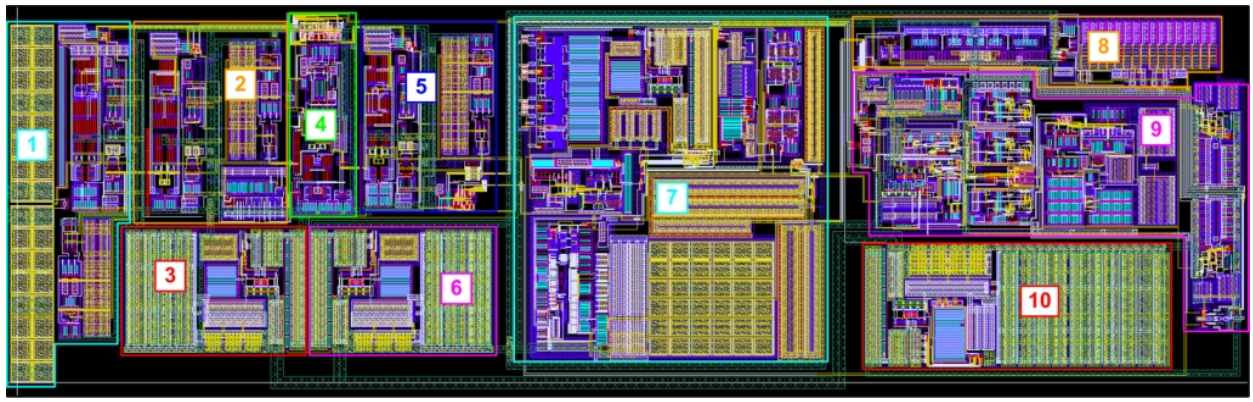

Figure 2: Intermediate-frequency amplifier layout

1. IFA 1st stage
2. IFA 2nd stage
3. IFA voltage regulator
4. IFA 3rd stage
5. IFA 4th stage
6. Voltage regulator for linear buffer with detector
7. Detector
8. IFA liner buffer
9. IFA digital buffer
10. Voltage regulator for digital buffer

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS BiCMOS 0.35 um
Status silicon verification
Area 1.22 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc_IFA} = 2.65 ÷ 3.15 V, V_{cc_BUF} = 1.8 ÷ 3.15 V, V_{cc_H} = 2.85 ÷ 3.15 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc_IFA} = V_{cc_BUF} = 2.7 V, V_{cc_H} = 3.0 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc_IFA}	-	2.65	2.7	3.15	V
	V_{cc_BUF}	-	1.8	2.7	3.15	
	V_{cc_H}	-	2.85	3.0	3.15	
Temperature operating range	T_j	-	-45	27	+85	°C
Frequency range	F_{IN}	-	0.8	-	25	MHz
Group delay time ripple	t_{del}	From 3 MHz to 9 MHz	-	3.3	4	ns
		From 6 MHz to 18 MHz	-	0.8	1	ns
Maximum gain	G_{max}	-	64	70	79	dB
Minimum gain	G_{min}	-	-2.8	-1	1.1	dB
Gain control range	ΔG_{IFA}	-	67	69	77	dB
Noise figure	NF_{IFA}	Gain more than 30 dB, input impedance 2 kOhm	-	9	-	dB
Input 1dB compression point	ICP	Minimal gain	-	-8.4	-	dBm
Input impedance	R	-	1590	2015	2560	Ohm
Output impedance	R_{out}	-	163	201	247	Ohm
Peak-to-peak voltage at the differential output	$V_{dif\_p\_p}$	For sinusoidal signal	190	199	215	mV
Output DC level	V_{IFA_dif}	-	1.5	1.85	1.95	V
ADC resolution	K	-	-	2	-	bit
Current consumption	I_{cc_dif}	-	-	6.4	8.2	mA
	I_{cc_ADC}	-	-	3.6	-	
Output logic-high leve (digital outputs)	V_{OH_dig}	-	$0.7V_{cc\_BUF}$	-	V_{cc_BUF}+0.25	V
Output logic-low leve (digital outputs)	V_{OL_dig}	-	-0.25	-	0.3	V
Stand-by current	I_{stb}	-	-	0.01	0.5	uA

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation