

PLL lock detector

SPECIFICATION

1 FEATURES

- TSMC018 SiGe 0.18 μ m
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. SelTime<1:0> and SelErr outputs set the lock monitoring period and the lock detector accuracy, respectively. The block is fabricated on TSMC018 SiGe 0.18 μ m technology.

4 STRUCTURE

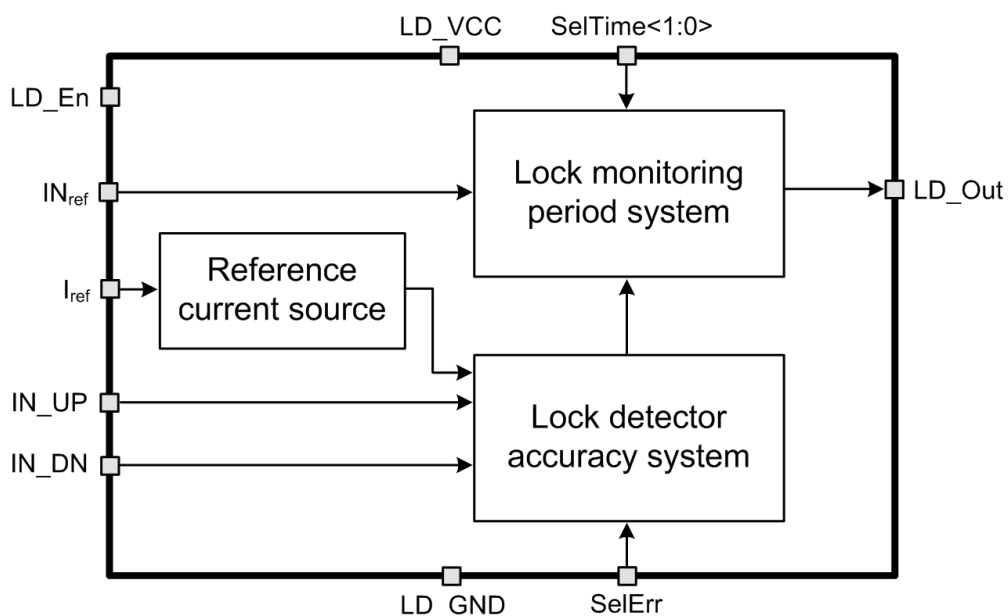


Figure 1: PLL lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
I _{ref}	IO	Reference current
IN_UP	I	CMOS input of PFD signal defined by the positive phase difference of VCO divided signal and reference oscillator signal
IN_DN	I	CMOS input of PFD signal defined by the negative phase difference of VCO divided signal and reference oscillator signal
IN _{ref}	I	Input of reference oscillator signal
SelTime<1:0>	I	Lock monitoring period
SelErr	I	Lock detector accuracy
LD_OUT	O	Lock indicator output
LD_En	I	Enable/disable lock detector
LD_VCC	IO	Supply voltage
LD_GND	IO	Ground

6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	73	μm
Width	120	μm

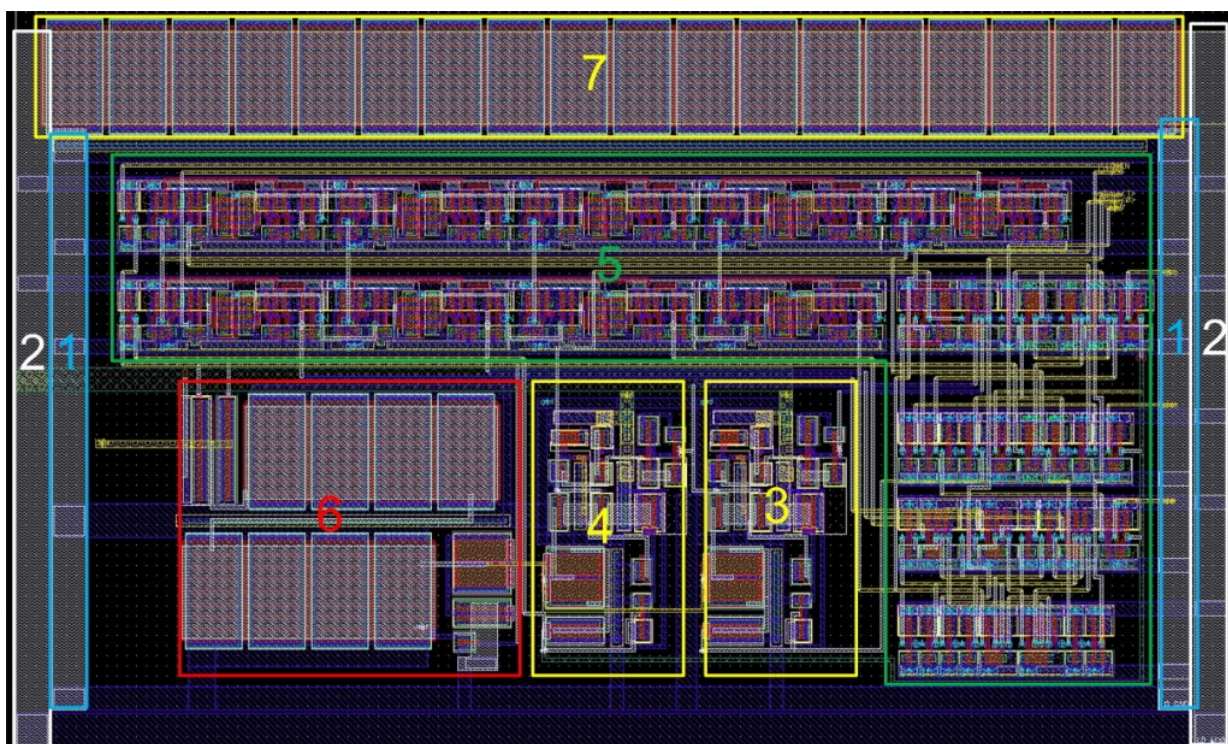


Figure 2: PLL lock detector layout view.

1. Ground bus
2. Supply voltage bus
- 3,4. Lock detector accuracy system
5. Lock monitoring period system
6. Reference current source with filters
7. Filters

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe
 Status _____ silicon proven
 Area _____ 0.009 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 2.8 \div 3.3$ V и $T = -40 \div +85$ °C. Typical values are at $V_{cc} = 3.15$ V, $T = +27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.8	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Peak-to-peak input voltage	$A_{in\ p-p}$	Fro inputs IN_UP, IN_DN, IN_ref	$V_{cc}-0.4$	V_{cc}	$V_{cc}+2.4$	V
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	$64 \times T_{ref}$	-	$512 \times T_{ref}$	µs
Lock detector accuracy	ACR	SelErr** = "0"	7.1	8	9	ns
		SelErr** = "1"	12.8	14.5	16.6	
Supply current	I_{cc}	-	75	95	110	µA
Stand-by current	I_{stb}	-	20	25	30	nA
Input logic-level high	V_{IH}	For digital inputs	0.7Vcc	-	$V_{cc}+0.25$	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Note:

* – F_{ref} – reference voltage.

** – SelErr – digital code setting the lock detector accuracy.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation