PLL lock detector

SPECIFICATION

1 FEATURES

- TSMC018 SiGe 0.18µm
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. SelTime<1:0> and SelErr outputs set the lock monitoring period and the lock detector accuracy, respectively.
The block is fabricated on TSMC018 SiGe 0.18µm technology.

4 STRUCTURE

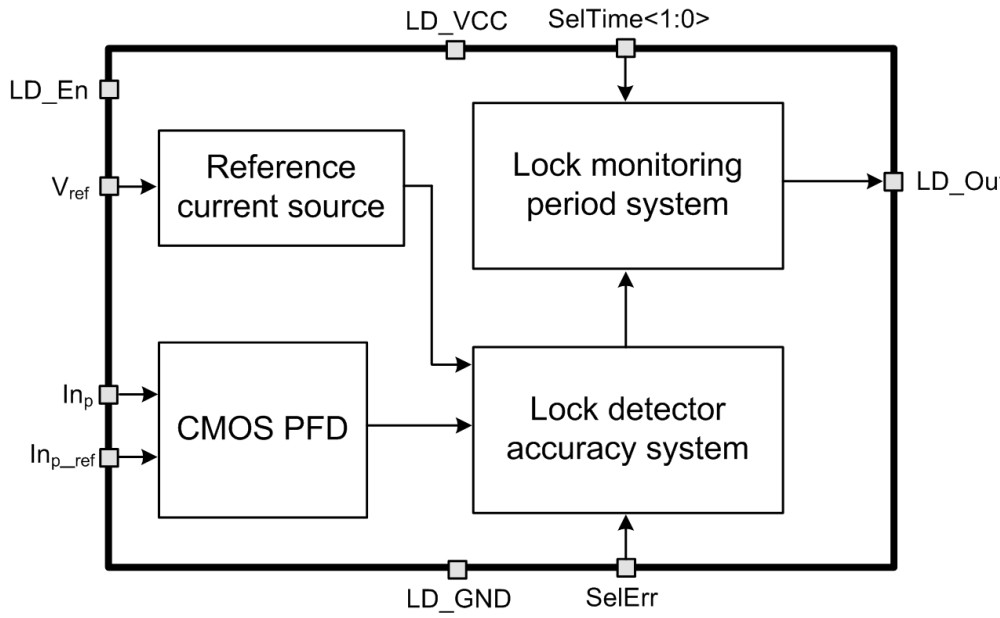

Figure 1: PLL lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
V_{ref}	IO	Reference voltage
IN_p	I	Input of VCO divided signal
IN_p_ref	I	Input of reference oscillator signal
SelTime<1:0>	I	Lock monitoring period
SelErr	I	Lock detector accuracy
LD_OUT	O	Lock indicator output
LD_En	I	Enable/disable lock detector
LD_VCC	IO	Supply voltage
LD_GND	IO	Ground

6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	67	µm
Width	122	µm

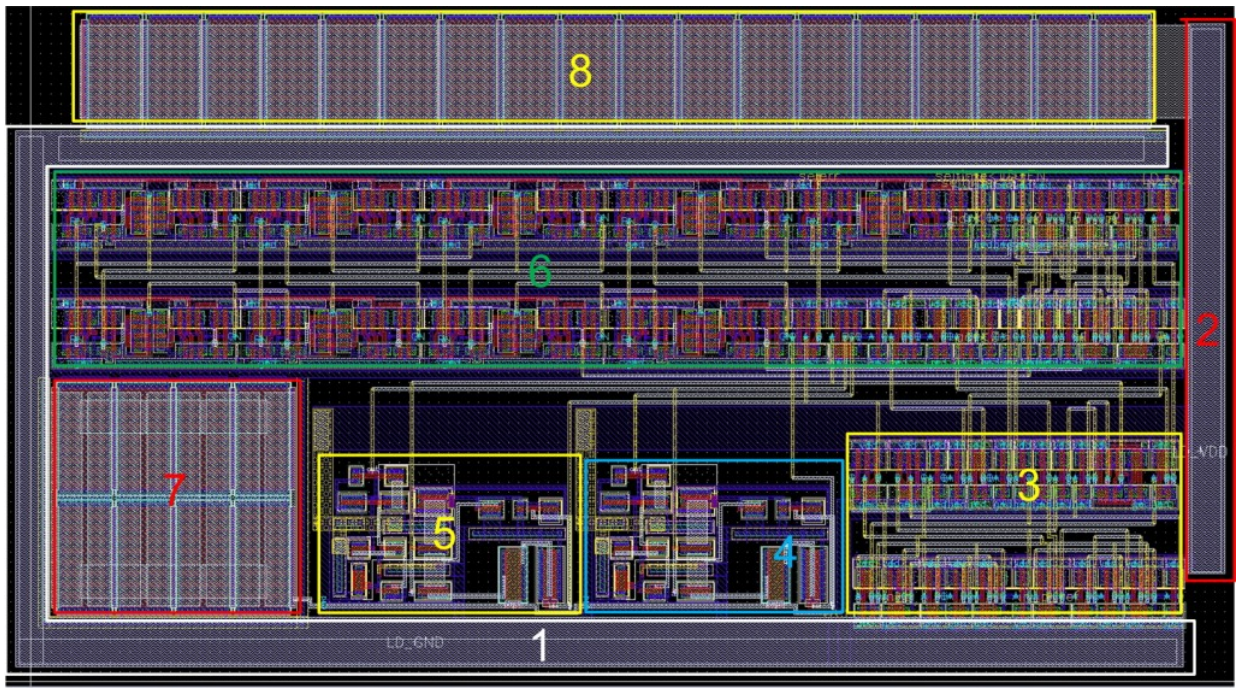

Figure 2: PLL lock detector layout view.

1. Ground bus
2. Supply voltage bus
3. CMOS PFD
4,5. Lock detector accuracy system
6. Lock monitoring period system
7. Reference current source with filters
8. Supply voltage bus filter

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC018 SiGe
Status silicon proven
Area 0.009 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 ÷ 3.6 V и T = -40 ÷ +85°C. Typical values are at V_{cc} = 3.15 V, T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.8	3.15	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	For inputs IN_p, IN_p_ref	V_{cc} -0.4	V_{cc}	V_{cc} +2.4	V
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	64×T_{ref}	-	512×T_{ref}	µs
Lock detector accuracy	ACR	SelErr** = “0”	5.5	6	7	ns
		SelErr** = “1”	10	12	13	
Supply current	I_{cc}	-	45	90	115	µA
Stand-by current	I_{stb}	-	20	25	30	nA
Input logic-level high	V_{IH}	For digital inputs	0.7 V_{cc}	-	V_{cc} +0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Note:
* – F_{ref} – reference frequaency.
** – SelErr – digital code setting the lock detector accuracy.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation