PLL lock detector

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra, X-FAB

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. LD_MP<1:0> and LD_ACR outputs set the lock monitoring period and the lock detector accuracy, respectively.

The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

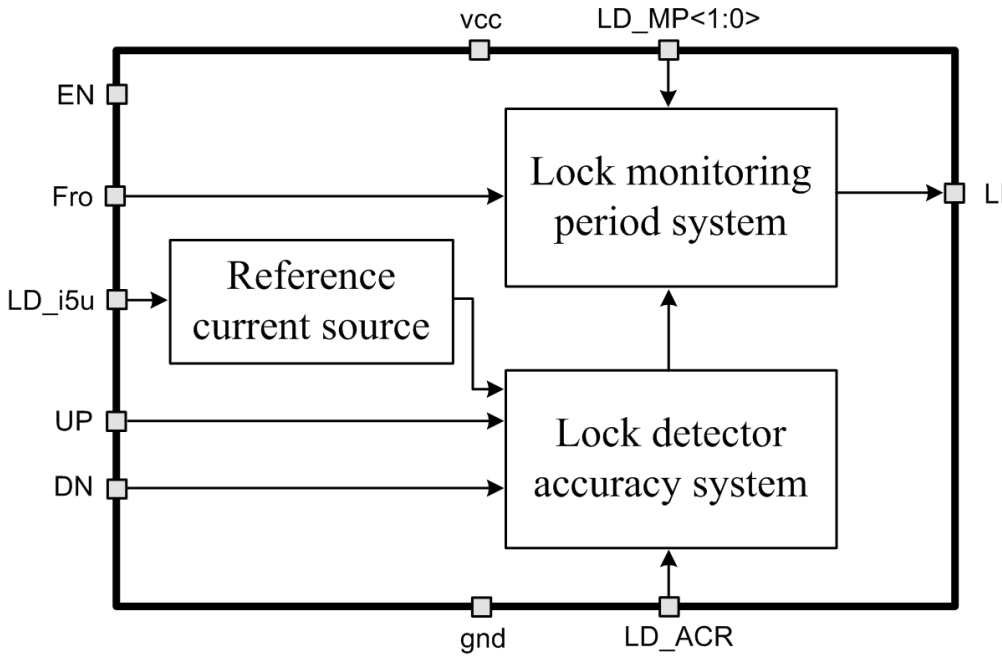

Figure 1: PLL lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
LD_i5u	IO	Reference current
UP	I	Input of PFD signal defined by the positive phase difference of VCO divided signal and reference oscillator signal
DN	I	Input of PFD signal defined by the negative phase difference of VCO divided signal and reference oscillator signal
F_{ro}	I	Input of reference oscillator signal
LD_MP<1:0>	I	Lock monitoring period
LD_ACR	I	Lock detector accuracy
LI	O	Lock indicator output
EN	I	Enable/disable lock detector
vcc	IO	Supply voltage
gnd	IO	Ground

6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	40	um
Width	190	um

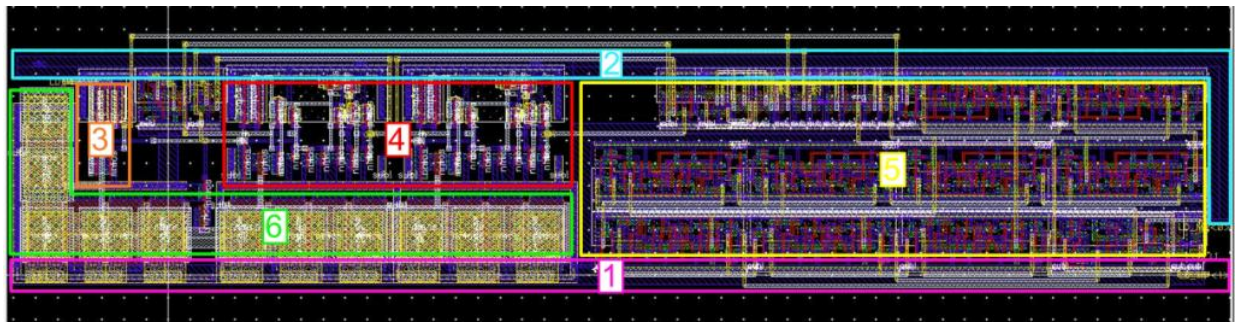

Figure 1: PLL lock detector structure.

1. Ground bus
2. Supply voltage bus
3. Reference current source
4. Lock detector accuracy system
5. Lock monitoring period system
6. Reference voltage filter capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 0.0076 мм^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.6 ÷ 2.75 V и T_a = -60 ÷ +125 °C. Typical values are at V_{cc} = 2.7 V, T_a = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.6	2.7	2.75	V
Operating temperature range	T_a	-	-60	27	125	°C
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	64×T_{ref}	-	512×T_{ref}	us
Peak-to-peak differential input voltage	$A_{in\ p\text{-}p}$	-	V_{cc} - 0.3	V_{cc}	V_{cc} +0.05	V
Lock detector accuracy	ACR	LD_ACR** = “0”	9.0	10.3	11.5	ns
		LD_ACR** = “1”	17.8	19.8	22.0	
Supply current	I_{cc}	-	24.0	26.5	29.7	uA
Stand-by current	I_{stb}	-	0.35	0.5	6.5	nA
Input logic-high level	V_{IH}	For digital inputs	0.7 V_{cc}	-	V_{cc} +0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Note:
*– F_{ref} – reference frequency.
** – LD_ACR – digital code defined lock detector accuracy.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation