

# PLL lock detector

## SPECIFICATION

### 1 FEATURES

- AMS035 BiCMOS
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

### 2 APPLICATION

- Phase-locked loop synthesizer

### 3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. SelTime<1:0> and SelErr outputs set the lock monitoring period and the lock detector accuracy, respectively. The block is fabricated on AMS035 BiCMOS technology.

### 4 STRUCTURE

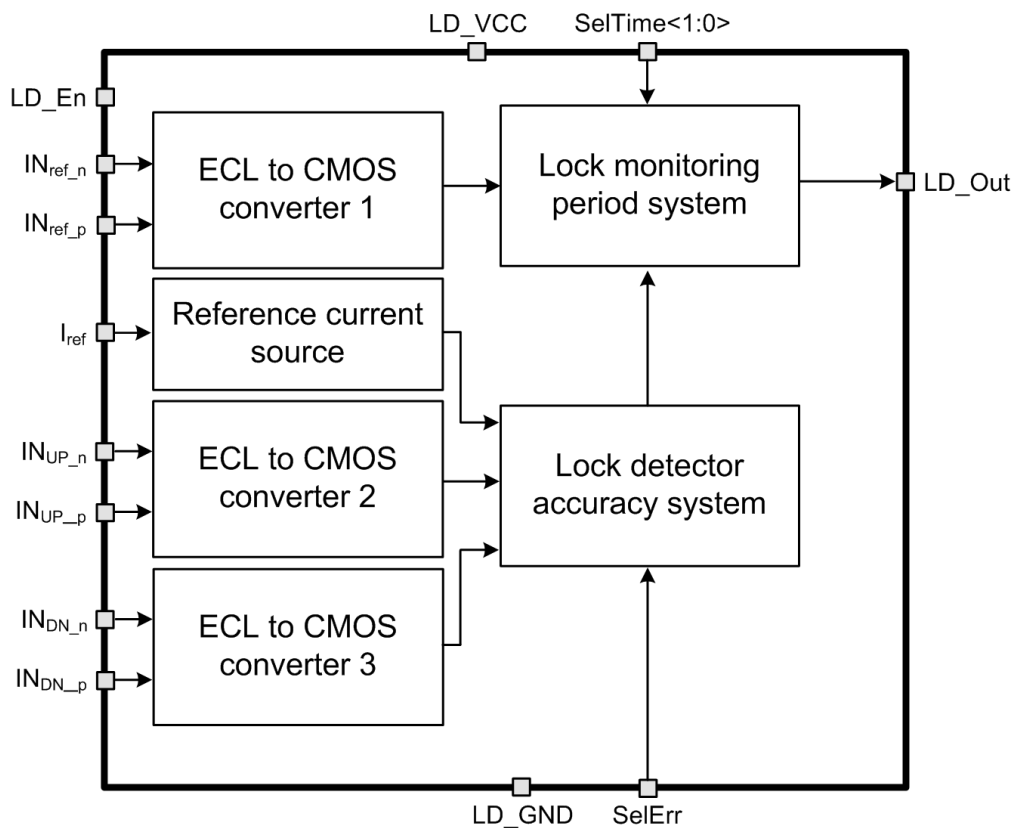


Figure 1: PLL lock detector structure.

## 5 PIN DESCRIPTION

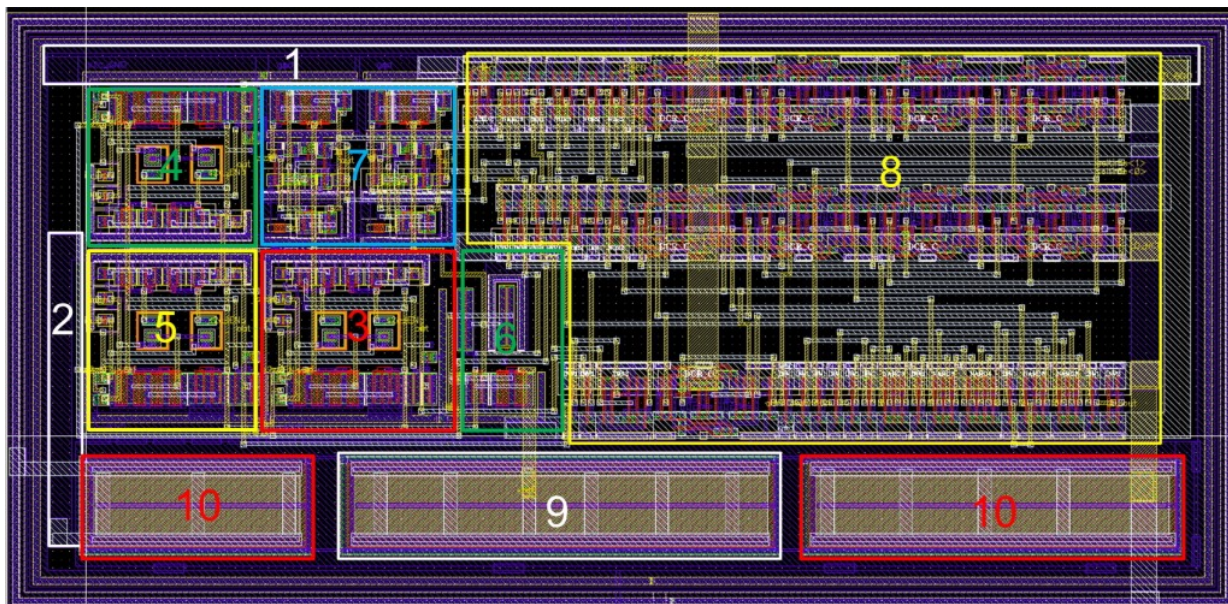
Name	Direction	Description
I <sub>ref</sub>	IO	Reference current
IN <sub>UP_n</sub>	I	Differential input of PFD signal defined by the positive phase difference of VCO divided signal and reference oscillator signal
IN <sub>UP_p</sub>	I	
IN <sub>DN_n</sub>	I	Differential input of PFD signal defined by the negative phase difference of VCO divided signal and reference oscillator signal
IN <sub>DN_p</sub>	I	
IN <sub>ref_n</sub>	I	Differential input of reference oscillator signal
IN <sub>ref_p</sub>	I	
SelTime<1:0>	I	Lock monitoring period
SelErr	I	Lock detector accuracy
LD_OUT	O	Lock indicator output
LD_En	I	Lock detector enable/disable
LD_VCC	IO	Supply voltage
LD_GND	IO	Ground

## 6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

**Table 1:** Block dimensions.

Dimension	Value	Unit
Height	100	$\mu\text{m}$
Width	210	$\mu\text{m}$



**Figure 2:** PLL lock detector layout view.

1. Ground bus
2. Supply voltage bus
3. ECL to CMOS inverter 1
4. ECL to CMOS inverter 2
5. ECL to CMOS inverter 3
6. Reference current source
7. Lock detector accuracy system
8. Lock monitoring period system
9. Reference voltage filter
10. Supply voltage bus filter

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ AMS035 BiCMOS

Status \_\_\_\_\_ silicon proven

 Area \_\_\_\_\_ 0.02 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

 The values of electrical characteristics are specified for  $V_{cc} = 3.0 \div 3.3$  V и  $T = -40 \div +85$  °C. Typical values are at  $V_{cc} = 3.15$  V,  $T = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{CC}$	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Peak-to-peak differential input voltage	$A_{in\ p-p}$	For inputs $IN_{UP\_n}$ , $IN_{UP\_p}$ , $IN_{DN\_n}$ , $IN_{DN\_p}$ , $IN_{UP\_n}$	0.2	-	2.0	V
DC operating point	$V_{op}$		$V_{cc} - 1.2$	-	$V_{cc} - 0.4$	V
Peak-to-peak differential output voltage	$A_{out\ p-p}$	-	-	$V_{cc}$	-	V
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	$64 \times T_{ref}$	-	$512 \times T_{ref}$	µs
Lock detector accuracy	ACR	SelErr** = "0"	6.0	8.0	9.0	ns
		SelErr** = "1"	13.0	15.0	18.0	
Supply current	$I_{cc}$	-	190	230	326	µA
Stand-by current	$I_{stb}$	-	0.3	0.5	150	nA
Input logic-level high	$V_{IH}$	For digital inputs	0.7V <sub>cc</sub>	-	V <sub>cc</sub> +0.25	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

Note:

 \* –  $F_{ref}$  – reference frequency.

\*\* – SelErr – digital code setting the lock detector accuracy.

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation