50mA capacitor-less LDO voltage regulator (output voltage 0.5V to 0.8V)

OVERVIEW

The 022GF_LDO_01 is capacitor-less Linear Regulator designed in GlobalFoundries 22FDX to generate internal supply voltage for core logic domain, SRAM array or RF/analog domain.

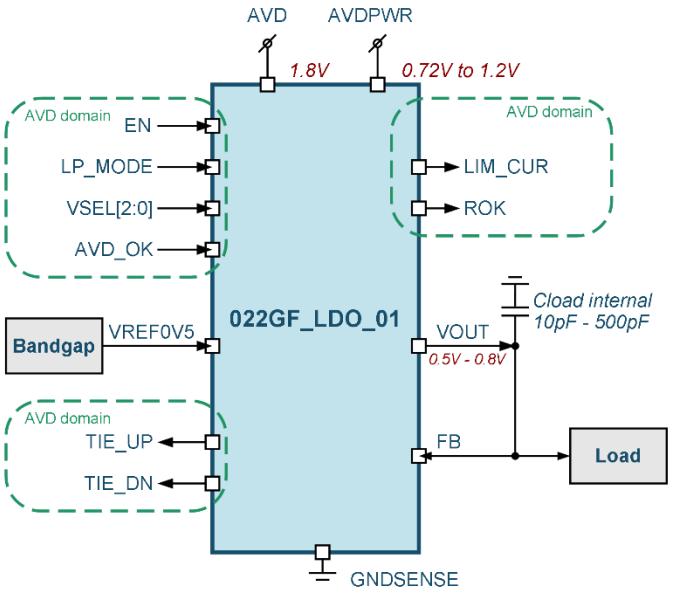
The LDO should be supplied by dual power supply, 0.72V to 1.2V voltage and 1.8V, and can generate programmable output voltage in the range of 0.5V to 0.8V.

The LDO requires an external voltage reference 0.5V and embeds voltage-to-current converter for biasing and logic control.

It features normal and low-power (LP) operating modes to adjust the amount of output current depending on the application requirements.

A current limiter signal notifies the system when the load current exceeds the limit and it starts limiting the output current.

A Regulation OK (ROK) signal inform the system that the LDO has completed its booting sequence and if its output is maintaining regulation for the current drawn by the load.



IP status: silicon proven. IP technology: GlobalFoundries 22FDX technology process.

Silicon area: 0.034mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Operating junction temperature	T_J	-		-40	25	125	°C
Power path input voltage range	V_{AVDPWR}	-		0.72	-	1.2	V
Input analog voltage range	V_{AVD}	-		1.62	1.8	1.98	V
Maximum output current	IMAX	Normal mode		-	-	50	mA
		LP mode		-	-	5	mA
Logic load capacitance	CLOAD	SoC internal		10	-	500	pF
Dropout voltage	VDROPOUT	$I_{LOAD} = I_{MAX}$		-	-	100	mV
External voltage reference	V_{REF}	-		-	0.5	-	V
Quiescent current	$I_{Q\_GNDSENSE}$	@AVD pin, Normal mode	I_{LOAD} = 5µA	-	5	-	µA
			I_{LOAD} = 5mA	-	63	-	
			I_{LOAD} = 50mA	-	65	-	
		LP mode	I_{LOAD} = 1µA	-	1	-	
			I_{LOAD} = 5mA	-	35	-	
Shutdown current	$I_{GNDSENSE\_SD}$	@GNDSENSE		-	7	135	nA
		@AVDPWR		-	35	5800	nA
LDO regulated output voltage. Programmed value	V_{OUT}	by default		-	0.5	-	V
		-		-	0.8	-	
Output voltage step	ΔV_{OUT_ADJ}	-		-	50	-	mV
DC accuracy*	ΔV_{OUT}	MC (Global+Local), including Line and Load Regulation	@0.8V output	-3.5	-	+3.5	%
			@0.5V output	-3.0	-	+3.0	%
Load transient amplitude	$\Delta V_{OUT}/V_{OUT}$	0.1*Imax to Imax in 50 ns, worst case over PVT, Cload=200pF		-	2.6	5.0	%
Power supply rejection ration	PSRR	DC, in Normal Operation mode	@AVD	-	-40	-	dB
			@AVDPWR		-40	-	
		F = 1MHz, in Normal Operation mode	@AVD	-	-15	-	dB
			@AVDPWR		-20	-	

Note: * DC accuracy of LDO without taking into account external voltage reference deviation